

SEU-TOLERANT SRAM DESIGN BASED ON CURRENT MONITORING ¹

F. Vargas², M. Nicolaidis

TIMA/INPG Laboratory
46, Av. Félix Viallet. 38000 Grenoble, France

Abstract

In this paper, we present a new technique to improve the reliability of SRAMs used in space radiation environments. This technique deals with the SRAM power-bus monitoring by using Built-In Current Sensor (BICS) circuits that detect abnormal current dissipation in the memory power-bus. This abnormal current is the result of a single-event upset (SEU) in the memory and it is generated during the inversion of the state of the memory cell being upset. The current checking is performed on the SRAM columns and it is combined with a single-parity bit per RAM word to perform error correction.

Keywords: Fault-tolerant SRAM; Single-Event Upset (SEU); Built-In Current Sensor (BICS); power-bus monitoring; error detection and correction techniques.

I. INTRODUCTION

At the present time, it is generally accepted that single-event upset (SEU) is a potential threat to the reliability of integrated circuits in space environment [1,2,3]. This subject is of considerable importance at present because SEU occurs in space applications due to the presence of cosmic rays. Heavy particles incident on memory systems produce a dense track of electron-hole pairs, and this ionization can cause transient upsets, also referred to as single-event upsets or soft errors [4,5,6]. It is interesting to note that Hubble Space Telescope has not only trouble with mirrors. The NASA's biggest space-based astronomical observatory is also struggling daily radiation-induced electronic failure. SEUs in a 1-Kbit low-power TTL bipolar random access memory are causing one of Hubble's crucial focusing elements to loose

data on a regular basis. Ironically, the chip has well-documented history of SEU failures. NASA officials knew about them before the craft was launched. Nothing was done, however, because Hubble's orbit takes it through relative benign radiation territory. It is only when the telescope passes through the heavily proton-charged South Atlantic Anomaly over Brazil that problems occur, and NASA engineers have developed a software solution to compensate for the errors [7].

In order to cope with this problem, this paper proposes an error detection/correction technique based on a combination of current monitoring and parity checking. Built-In Current Sensors (BICSs) monitor the RAM columns to detect the abnormal current produced by single-event upsets and localize the affected column. A parity check allows to localize the affected word and thus allowing error correction. With respect to Single Error Correcting/Double Error Detecting (SEC/DEC) codes [16], the new technique requires drastically lower area overhead, simpler encoding/decoding algorithms and also has the advantage of zero fault latency time. On the other hand, two-dimensional parity codes [16] require similar area overhead as the new technique, but they involve speed degradation for the write operation (for maintaining the integrity of the columns parity) and introduces fault latency.

II. SINGLE-EVENT UPSETS

In a CMOS static memory cell, the nodes sensitive to high-energy particles are the drains of off-transistors. Thus, two sensitive nodes are present in such a structure: the drains of the p-type and the n-type off-transistors.

When a single high-energy particle (typically a heavy ion) strikes a memory cell sensitive node, it will loose energy via production of electron-hole pairs, with the result being a densely ionized track in the local region of that element [8]. The charge collection process following a single particle strike is now described. Fig. 1 shows the simple example case of a particle normally incident on a reverse-biased n⁺p junction, that is, the drain of n-type off-transistors. Charge collection occurs by

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three processes which begin immediately after creation of the ionized track: drift in the equilibrium depletion region, diffusion and funneling. A high electric field is present in the equilibrium depletion region, so carriers generated in that region are swept out rapidly; this process is called drift. Carriers generated beyond the equilibrium depletion region width, more specifically, the charge generated beyond the influence of the excess-carrier concentration gradients, can be collected by diffusion. The third process, charge funneling, also plays an important role in the collection process. Charge funneling involves a spreading of the field lines into the device substrate beyond the equilibrium depletion width. Then, the charge generated by the incident particle over the funnel region is collected rapidly. If the charge collected, Q_d , during the occurrence of the three processes described before is large enough, greater than the critical charge Q_c of the memory cell, then the memory cell flips, inverting its logic state (the critical charge Q_c of a memory cell is the greatest charge that can be deposited in the memory cell before the cell is corrupted, that is, its logic state is inverted). Fig. 1b shows the resulting current pulse shape that is expected to occur due to the three charge collection processes described

the p-substrate (resp. n-well), for the case of an n-well technology, for instance.

Note that this current pulse is not the abnormal current that will be monitored by BICS. This current pulse (shown in fig. 1) flows between the reverse-biased depletion region of a transistor and the substrate (or well) and it is the result of the collection of the charge generated during the particle strike in the material. While the abnormal transient current monitored by BICS is measured in the power-bus and it is the result of the state inversion of the memory cell being upset (that is, during the switching of the memory cell, when n- and p-transistors are ON at the same time). Depending on the quantity of the charge deposited, the 5V or the 0V representing the information stored in the drain of the transistor upset is temporarily degraded, being discharged towards 0V or charged towards 5V, respectively. The resulting degradation of the signals in the gates of the cross coupling inverters of the memory cell generates a transient current in the power-bus of the memory. This current is proportional to the collected charge. Then, if a Built-In Current Sensor (BICS) is placed between the memory cell being upset and the power-bus of the memory, it will be possible to detect this current transient.

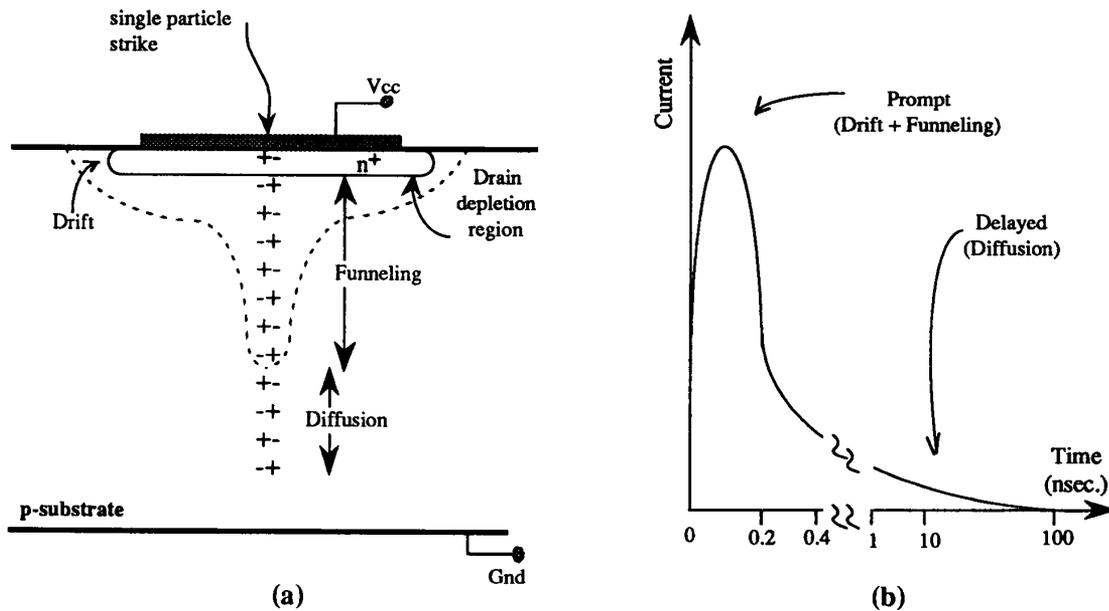


Fig. 1. Illustration of the charge collection mechanism that cause single-event upset: (a) particle strike and charge generation; (b) current pulse shape generated in the n+p junction during the collection of the charge.

above. This current pulse is generated between the reverse-biased n^+ (resp. p^+) drain depletion region and

III. BICS FOR UPSET MONITORING IN SRAMs

Traditional BICS [9,10,11,12,13,14,15] are used to monitor the static current dissipation (I_{ddq}) on the circuit, and thus they are synchronized by the system clock. On the other hand, SEUs may occur at any time and are asynchronous to the system clock. Thus, unlike to traditional BICSs, the present application requires to use an asynchronous BICS.

strength and duration of this pulse are large enough, the latch will be set up via transistors T11 and T12: these transistors are turned on for a while, due to the positive pulse on the BICS output, loading the parasitic capacitances (the gates of the cross-coupled inverters of the latch). Also the positive pulse on the BICS output turns off transistor T13 and isolates the latch from V_{cc} , resulting in a faster set up of the latch.

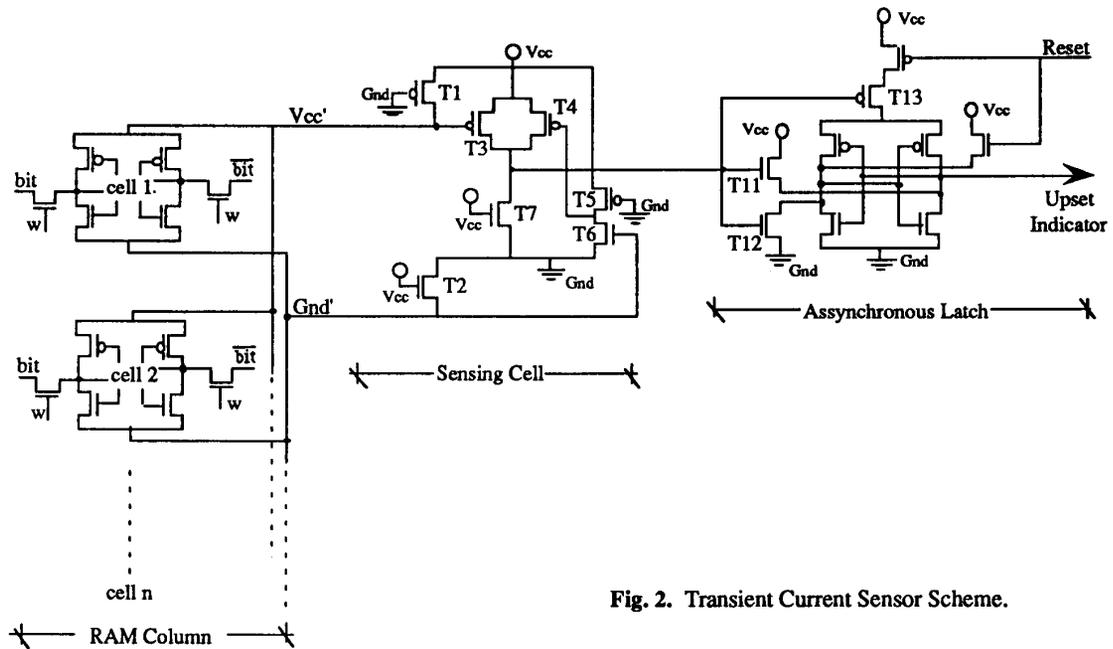


Fig. 2. Transient Current Sensor Scheme.

Fig. 2 shows the proposed current sensor, which is composed by a sensing cell followed by an asynchronous latch. This BICS is placed between the memory cells belonging to the same column and the power-bus (V_{dd} and Gnd) of this column, as shown in fig. 3. In the absence of current in the virtual power-bus, V_{cc}' and Gnd' , the voltage level on the gate of transistor T3 is V_{cc} (via transistor T1) and the one on the gate of T6 is Gnd (via T2), driving the BICS output to 0V (via transistor T7). When an upset is produced, we have the following two situations:

- if the upset is due to a particle which charges the drain of the p-type transistor that is off, then, the gate of T6 is charged to a voltage v_c ($v_c > 0$);
- if the upset is due to a particle which discharges the drain of the n-type transistor that is off, then, the gate of T3 is discharged to a voltage v_d ($v_d < 5V$).

In both cases the voltage level on the BICS output is increased, producing a positive pulse (see fig. 4). If the

The keys for making the present technique practical are:

- a) when the collected charge, Q_d , produced by a particle strike is large enough to provoke an upset, the generated power-bus transient current is detected by the BICS.
- b) the BICS sensitivity is calibrated with some security margins (e. g. detection of collected charges of 40% lower than the critical charge Q_c) to guarantee that SEUs cannot escape detection.
- c) the power-bus transient current generated during a read or a write operation is not detected by the BICS. Note that if condition c) does not hold during the write or the read operations (or both), the technique can be still used, but the BICS connected to the column involved by such an operation must be inhibited. In this case, the memory cells cannot be monitored permanently and the efficiency of the technique is reduced.
- d) when an SEU coincides with a write or a read operation, it is still detected by the BICS.

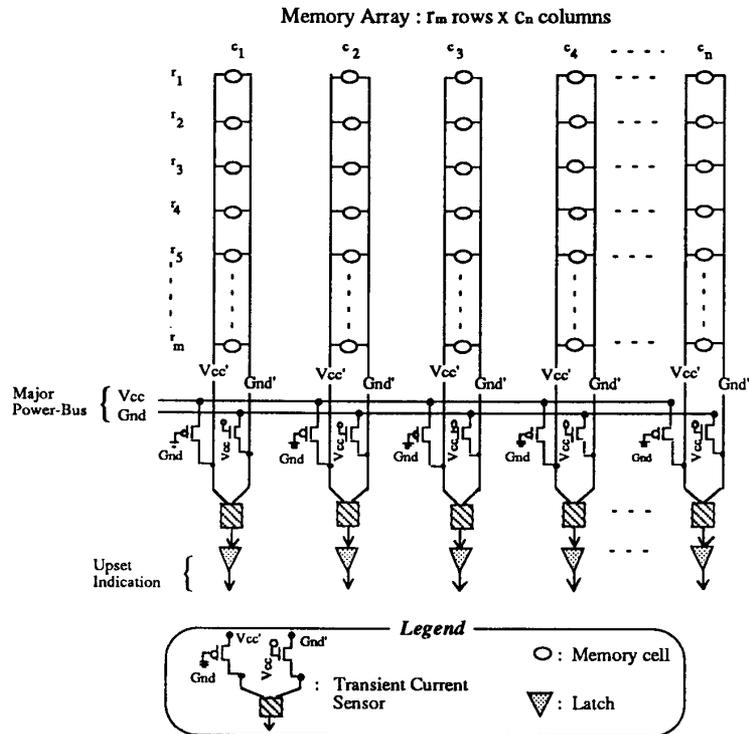


Fig. 3. General structure of an SRAM using the BICS shown in Fig. 2 to detect SEU-induced power-bus transient currents.

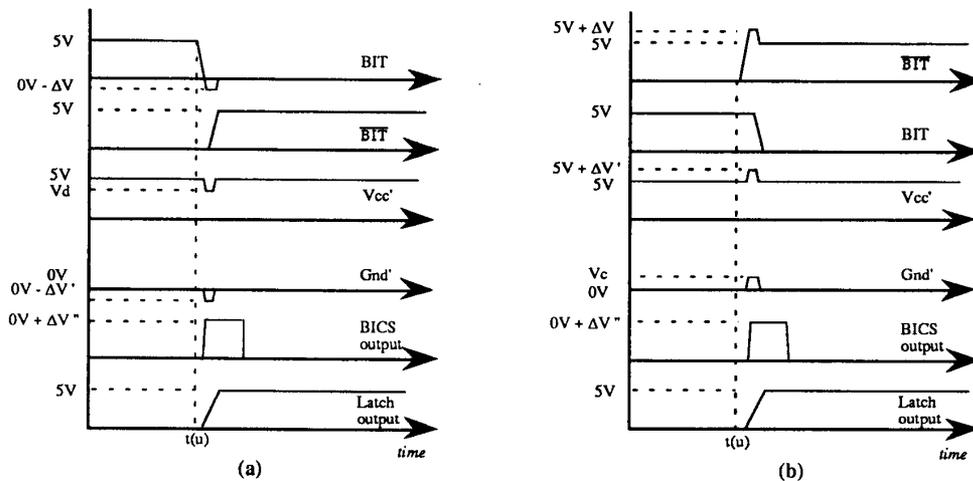


Fig. 4. Timing of the abnormal power-bus transient current detection. $t(u)$ is the upset occurrence instant.
 (a) upset from '1' to '0': a particle strikes the '1' side, that is discharged, which results in the charge of the '0' side;
 (b) upset from '0' to '1': a particle strikes the '0' side, that is charged, which results in the discharge of the '1' side.

Simulation experiments and sizing of the BICS components were used to achieve conditions a), b), c) and d). They will be described in the next section.

IV. SIMULATION RESULTS

In this section, it is presented some SPICE simulation results of our approach. Based on these results, the performance and limitations of the SEU-tolerant scheme are estimated, discussed and a modification of the transient current sensor shown in fig. 2 is proposed. In the end of this section, the final version of the BICS is presented.

To perform SPICE simulations we have first to compute the critical charge Q_c , that is, the minimal collected charge resulting in an upset. The current involved by an upset flows between the n-type off-transistor drain and the substrate, or the p-type off-transistor drain and the n-well. Thus, to perform SPICE simulation we connect to the sensitive node (drain of the above n- or p-off-transistors) a current generator simulating the curve of fig. 1b (according to a technique described in the literature [16,17,18]). This current can be approximated by the simpler curve of fig. 5. Then, we first determine the minimal current involving an upset (it corresponds to the critical Q_c). We start with a curve that does not involve upset and we increase gradually I_{max} until a value I_c that creates an upset. The critical charge Q_c is computed by taking the integral ($Q_c = \int I_c dt$) over the curve of fig. 5 with I_{max} equal to I_c . In these simulations we have considered a memory cell using inverters with minimal size, and we have obtained $Q_c = 0.45pC$ for a charge collected in the drain of the p-type off-transistor of the cell, and $Q_c = 0.20pC$ for a charge collected in the drain of the n-type off-transistor.

The technique of the current generator described before can also be used to simulate the behavior of the BICS under various values of the collected charge and/or I_{max} in the sensitive nodes of the cells.

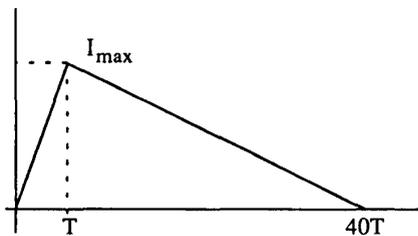
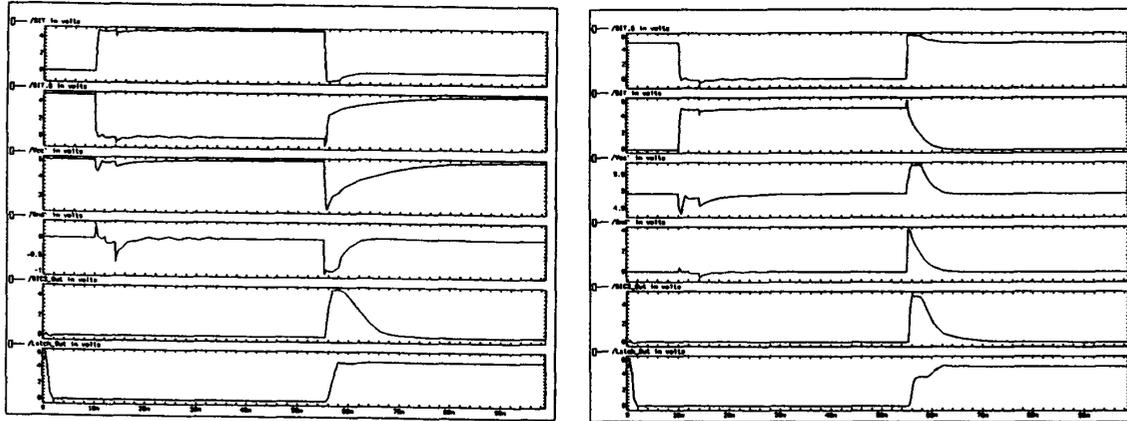


Fig. 5. Waveform used in SPICE to simulate an upset in the sensitive node of a memory cell.

SPICE simulations are used to design a BICS which meets conditions a), b), c), and d) of the previous section and whose results are given in figures 6 to 10:

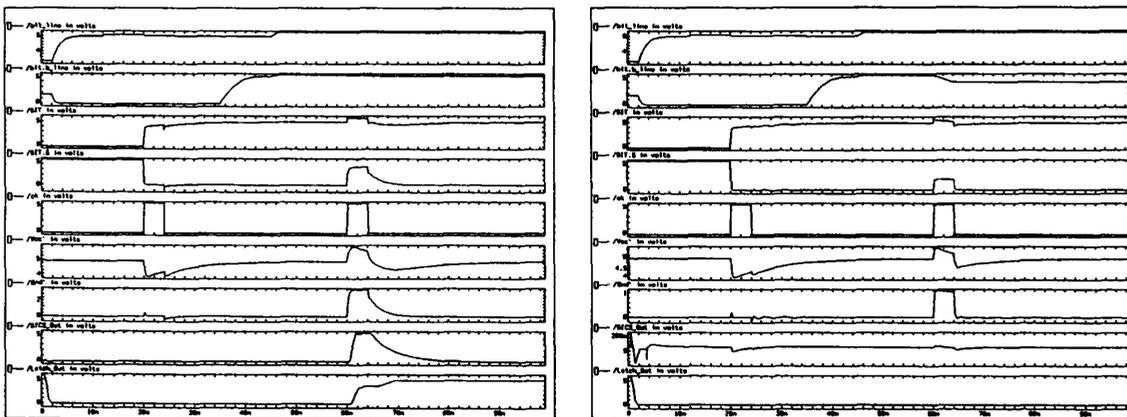
a) To meet condition a), two situations must be taken into account. The one concerns the case that the particle strike generates the minimal collected charge that involves cell upset (Q_c). The second situation concerns the case of a high energy particle that creates a large collected charge. Surprisingly the second situation can also escape detection. This is due to the fact that for collected charges close to Q_c the state of the memory cell changes slowly, swinging from 0V and $V_{cc}/2$ and from Gnd and $V_{cc}/2$. Then, the memory cell slowly changes its state, for deposited charges greater than Q_c , or then it slowly returns to its initial state, for deposited charges smaller than the critical one. All these slow transitions generate large current transient of long duration in the virtual power-bus of the memory, and can be detected by the BICS. On the other hand, for large collected charges, many times greater than Q_c , the affected memory cell changes its state very fast, generating a smaller transient current of shorter duration in the virtual power-bus of the memory. This resulting short current in the virtual power-bus can go undetected by the BICS. Then, the BICS must also be specified to detect this short current pulse. Based on this understanding of the abnormal current dissipation mechanisms, the BICS is designed to meet condition a). Fig. 6 concerns the case of a large collected charge (the worst-case). In order to be sure that the sensor is able to detect all the range of high energy particles occurring in actual environments, we have simulated upsets with a current source that generates a huge current of 0.1A ($\approx 280pC$ of collected charge). These values are not realistic, being exaggerated figures-of-merit, but are very useful if we want to detect all incidents involving upsets. Fig. 6a and 6b show the corruption from '1' to '0' and from '0' to '1' of the information stored in the memory cell, followed by the outputs of the BICS and the latch. In this fig. and in figs.7 and 9, bit_line, bit.b_line are the bit and \bar{bit} lines of the memory; BIT and BIT.B are the cross coupling inputs/outputs of the memory cell inverters, where the information is stored; ck is word enable for the memory cell; Vcc' and Gnd' are the power-bus of the RAM column; BICS_Out and Latch_Out are the outputs of the BICS and the latch, respectively. Note finally that the critical device of the BICS is transistor T2. The resistance of this transistor (implemented in the present case with a factor $W/L = 1/7$) involves a voltage drop and decreases the speed of read operations. This problem is addressed in the discussion of conditions c) and d).



(a)

(b)

Fig. 6. Timing of the abnormal power-bus transient current detection. 55ns is the upset occurrence instant.
(a) upset from '1' to '0': a particle strikes the '1' side, that is discharged, which results in the charge of the '0' side;
(b) upset from '0' to '1': a particle strikes the '0' side, that is charged, which results in the discharge of the '1' side.



(a)

(b)

Fig. 7. SPICE waveforms for a write and a read operation in the memory cells. **(a)** false alarm generated by the BICS during the read operation; **(b)** correct behavior of the BICS.

b) This condition guarantees detection of all SEUs, but creates conditions for false alarms (some incidents which do not produce SEUs, but whose collected charges are close to the critical charge Q_C , will be detected). These alarms will activate the error correction procedure, but the parity checking will not indicate error detection and no correction will be performed. Thus, the system will continue to operate with correct data. Simulation results have shown that the designed BICS has a comfortable security margin, since it detects current generated from collected charge of 0.12pC , while Q_C is 0.20pC .

c) This condition is met easily for write operations since the bit lines impose the new '0' and '1' values to the two sides of the memory cell. The memory cell is found close to the new equilibrium state and the duration of the transition of the cell is short and goes undetectable by the BICS (see the BICS output in fig. 7a, where the first pulse of ck , $t=20\text{ns}$, corresponds to a write operation in the cell). On the other hand, during a read operation, both the '0' and the '1' sides of the memory cell are connected to the precharged bit lines. The '0' side will be charged to some value greater than $0V$. Since the capacitance of the bit lines is large, the voltage of the '0' side can be increased to the analog domain (i. e., both the p- and n-transistors of the inverter driven by this node are on the ON-state) resulting on current dissipation. The duration of this phenomenon can also be large, inducing the BICS to produce a false alarm. In this case, the BICS cannot be calibrated both to be sensitive to the SEUs and insensitive to the current generated by a read operation (see the BICS output in fig. 7a, where the second pulse of ck , $t=60\text{ns}$, corresponds to a read operation in the cell). In order to overcome this problem, we added a transistor (T8) in parallel with transistor T2, as shown in fig. 8. Transistor T8 is turned ON only during read operations. By sizing T8 to have a resistance sufficiently low, false alarms are avoided during read operations (see the BICS output in fig. 7b, where the second pulse of ck , $t=60\text{ns}$, corresponds to a read operation in the cell). The simulation has been given for a capacitance of the virtual power-bus (V_{cc} and Gnd) corresponding to a column with 256 cells.

d) Suppose that a particle strikes the node of a cell being written. This condition holds easily, since during the write operation the memory cell is being written from both sides by the very large capacitances of the bit lines. Then, if a particle strikes one of the sensitive nodes of the memory cell, it must deposit a charge greater than the critical charge of the cell plus the critical charge that corresponds to the capacitance of the bit line itself that is driving the sensitive node (which is not realistic). This implies that if a heavy ion strikes the sensitive node of a memory cell while this cell is being

written, it does not produce upset. This is shown in the simulation of fig. 9a (see the BICS output, where the first pulse of ck , $t=20\text{ns}$, corresponds to a write operation in the cell). On the other hand, when a particle strikes another cell that the one being written, then the current produced by the upset is added to the one produced by the write operation and the incident is detected comfortably. On the other hand, due to the activation of the low-resistance transistor T8, the BICS detection may be prevented when a read operation coincides with an SEU. To avoid it, T2 and T8 must be sized to calibrate the BICS sensitivity on a current level between the current generated by the read alone and by the current generated when the read operation coincides with an incident which creates a collected charge $Q_C - d$ (d is the security margin). The simulation results obtained after adequate sizing of transistor T8 are as shown in fig. 9b, where it is possible to see that the BICS is able to detect a simultaneous upset of a memory cell with a read operation of another cell, both cells belonging to the same column of the memory (see the BICS output, where the second pulse of ck , $t=60\text{ns}$, corresponds to a read operation in the cell). As for condition c), these simulation results have been given for the virtual power-bus (V_{cc} and Gnd) capacitance corresponding to a column with 256 cells. The size of transistor T8 used in the simulation corresponds to a factor $W/L = 4$. This corresponds to a low resistance and it allows fast read of the cell.

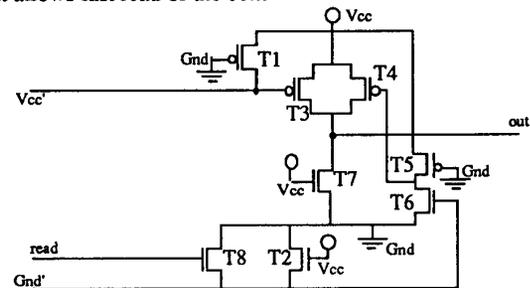


Fig. 8. Final version of the transient current sensor.

Fig. 10 shows the layout of the BICS and the latch. This layout was realized using CMOS double metal $1.5\mu\text{m}$ technology and the obtained cell was incorporated to our library. The design of an SRAM using BICS cells is presently under development.

IV.1. Speed considerations

Inserting transistors on the current path (like transistors T1 and T2) could decrease the memory speed. Fortunately, in opposition to the standard BICS applications where the BICS has to drive the current produced by many gates at a time, in the present

application only one cell per column is read or written at a time. Thus the current level to be driven by the BICS is low and the speed degradation cannot be excessive. More detailed analysis of the circuit behaviour shows that the speed degradation is low :

For read operations both the sides of the cell are connected to the precharged bit lines. The voltage level of the bit line connected to side with 0 logic value will be decreased to a value between Vdd and Ground, while the voltage level of the second bit line is not affected. Thus,

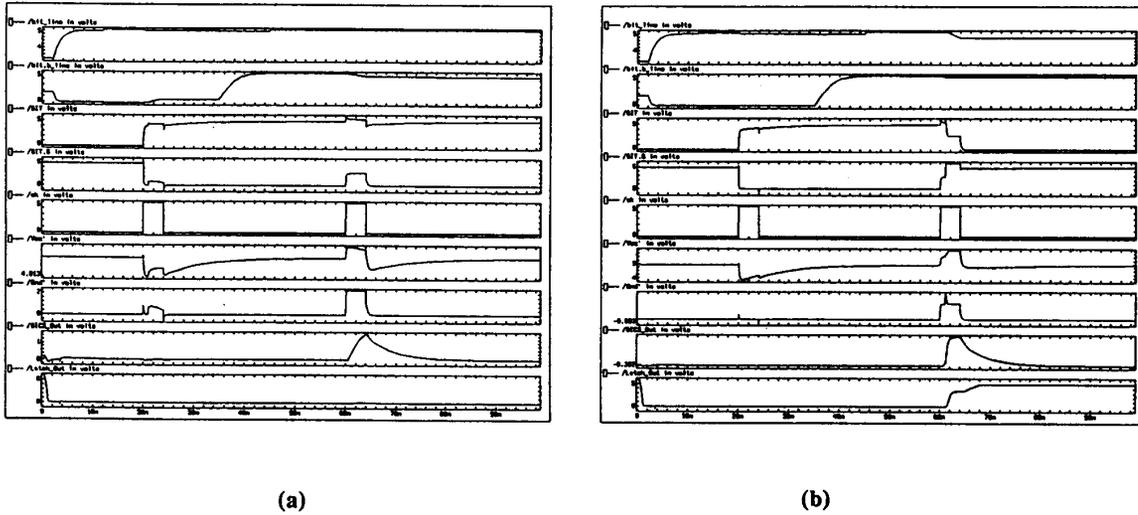


Fig. 9. SPICE waveforms for: (a) simultaneous occurrence of an SEU and a write operation in the memory cell. (b) simultaneous occurrence of an SEU and a read operation in the memory cell.

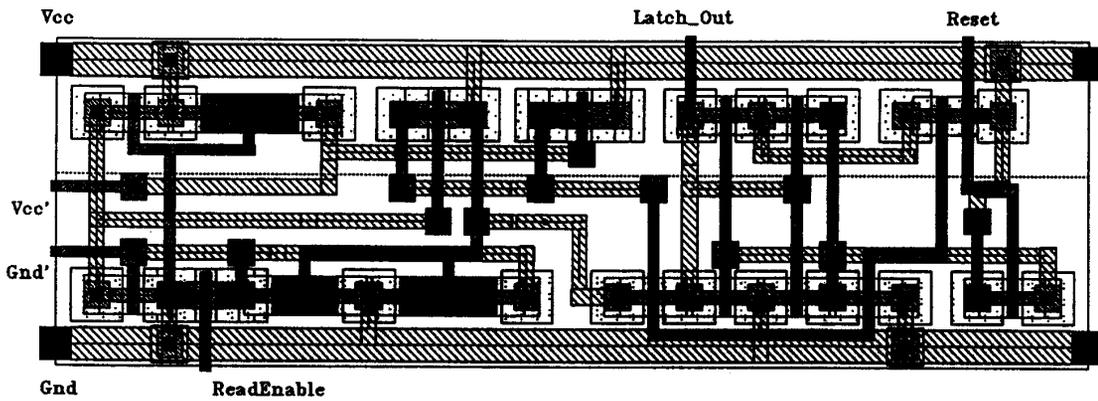


Fig. 10. Layout for the BICS and latch. Total cell area: 160X50 (8000 μ m²).

the critical current path connects the first bit line to the Ground and passes through the n-transistor controlled by the word line (w), the n-transistor of the cell inverter and the transistor inserted on the path by the BICS. Fortunately, in order to reach the conditions for the BICS we turn ON transistor T8 during the read operations. In the design described above this transistor has a factor $W/L = 4$ while the two first transistors (i.e. the transistor of the inverter and the one of the word line) have a factor $W/L = 1$. Thus inserting the BICS will increase the resistance of the critical path at only 12,5 % and the speed degradation is low. Furthermore, this degradation can be eliminated by slightly increasing the width of the two first transistors.

For write operations the critical case is when the cell has to change its state. We have to consider two phases for this case. During the first phase the bit line imposes the new values (0,1 or 1,0) to the two sides of the cell and brings the cell state close to the new equilibrium state (0,1 or 1,0). During this phase the currents which flow from the bit lines to Vdd and Ground (through the paths that pass by the memory cell) resist to the state transition. Thus increasing the resistance of these paths (due to the transistors T1, T2 inserted by the BICS) increases the speed of this phase. During the second phase the voltage values of the two sides of the cell are close to the new equilibrium state. In this case the above currents help the cell to reach the new equilibrium state. Thus the resistance increasing involved by the BICS will decrease the speed of this phase. The two above phenomena cancel each other and there is no significant speed degradation for write operations. Furthermore, since write operations are faster than read ones, slight speed degradation for write operations is not a drawback. SPICE simulations confirm this analysis.

V. ERROR CORRECTION PRINCIPLE AND COMPARISON

In order to perform error correction, the BICS monitoring is combined with a parity check. To do that, a parity bit is added to each RAM word. Then, when some BICS indicates the occurrence of upset, the error correction procedure is activated. The memory words are read one after another and their parity is checked. When a parity error occurs for a word, the bit position in the word corresponding to the BICS which indicates the upset occurrence is inverted. On the other hand, when a false alarm occurs, there is no error in the RAM and correction must not be performed. This requirement is met since in this case the parity checking will not detect any error and no correction is performed.

Note that this technique will introduce some interruption of the normal operation mode each time an error is detected. The duration of this interruption can be decreased by splitting the power lines of each column into

smaller parts and using a BICS to monitor each part. Another possibility is do not to correct the error as soon as it is detected but to wait until that a read operation of the normal operation mode accesses the erroneous word. In this case, there is not at all interruption of the normal operation mode. The drawback of this technique is that it may introduce a large latency between the SEU occurrence and the error correction.

Note also that double errors produced by SEUs are always detected by the BICS, but they cannot be corrected (e. g. if the double error affects the same word there is no detection by the parity checking). However, the probability of occurrence of two simultaneous upsets is low. In practice, in memories protected by error correcting codes, most of the double errors are due to the latency of the error involved by a first upset. So that a second one may occur before the first error is corrected. The scheme presented here has therefore the decisive advantage to detect upsets immediately as they occur and thus it avoids this situation.

The new technique has also some other advantages. In comparison with a memory scheme using a Hamming Single Error Correction/Double Error Detection (SEC/DED) code, the hardware overhead is drastically lower. Consider for instance an SRAM of 1Kbytes (16-bit words). The SEC/DED code requires 6 check bits per word, corresponding to $6/16 \cong 37,5\%$ overhead. On the other hand, our technique using a parity bit per word and a BICS per column of 256 cells requires $1/16 \cong 6,2\%$ overhead for the parity bit and $17/(256 \times 6) \cong 1,1\%$ transistor count overhead for the BICSs (17 transistors per BICS).

As concerning hardware complexity for the encoding/decoding circuitry, the new technique requires a parity checker/generator and also a counter (for addressing all the RAM cells during the error correction procedure). The SEC/DED code requires a Hamming code checker/generator and a decoder to localize the faulty bits from the value of the syndrome. The hardware of the encoding/decoding circuitry is of similar complexity. Finally, the new technique has the drawback that the correction procedure is more time consuming since it requires to read the contents of the whole RAM. However, this procedure is realized only when an upset occurs and it does not compromise the system performances. Furthermore, if one desires to reduce the time required for error correction, one can divide the power buses of the RAM columns into smaller sections and then use a BICS to monitor each section. Thus, when an upset is detected by a BICS only the rows of the corresponding section have to be read.

Concerning the scheme using a two-dimensional parity code [16], (a parity bit per word and a parity bit per

column), both the techniques require to read the contents of the whole RAM for performing error correction. The hardware overhead is similar since the two-dimensional code requires a parity bit per word and also a memory cell per column for storing the column parity (6 transistors) plus a flip-flop and an XOR gate (30 transistors) for performing the column parity computation during the correction procedure. However, the two-dimensional code has the drawback that each write operation must be preceded by a read one in order to recompute the column parity, resulting in a significant degradation of the write operation speed. Of course, as explained previously, the new technique has also the advantage of detecting upsets with zero latency.

It is also to note that another important application of the new technique concerns error correction in Content Addressable Memories (CAMs). In this case, the use of error correcting codes cannot ensure fault tolerance for the tag part of the CAM. In fact, if a bit is flipped in some tag location, then an incorrect mismatch will be produced when the address is equal to the correct content of this location. Since in CAMs each tag location possesses its own comparator and the address is compared in parallel with the contents of all the tag locations, using error correcting codes does not allow to tolerate errors in the tag part unless all the tag locations are read before each operation (resulting on unacceptable performance degradation) or unless each tag location possesses its own control code circuit (resulting on unacceptable hardware overhead). On the other hand, the technique presented in this work can be used to detect SEUs occurring in the tag part of the CAM in the same way as for RAMs. Then, modifying the tag part in order to enable read operations and using a parity bit per tag location will allow to correct the error in the same way as for RAMs. Thus, the present technique is the unique one allowing to design SEU-tolerant CAMs.

VI. CONCLUSIONS

A new technique for detecting and correcting single-event-upset-induced errors in RAMs has been presented. The technique uses a Built-in Current Sensor per RAM column in order to detect the occurrence of SEU and to localize the affected column. A parity bit per RAM word is added to localize the affected word and to perform the error correction. Detailed simulations have been given to check that we can meet all the conditions required for the technique to be effective. In comparison with techniques using error correcting/detecting (SEC/DED) codes, the new technique has several advantages such as drastically lower area overhead and zero latency time. Also, the proposed technique is the unique known technique (excepting TMR) that achieves SEU-tolerance for CAMs.

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