On Latching Probability of Particle Induced Transients in Combinational Networks*

Peter Lidén, Peter Dahlgren, Rolf Johansson, Johan Karlsson

Department of Computer Engineering, Chalmers University of Technology
S-412 96 Gothenburg, Sweden

Abstract

The question to what extent particle induced transients in combinational parts of a circuit propagate into memory elements is addressed in this paper. An experimental method is presented in which the proportion of bit flips originating from heavy-ion hits in combinational logic is determined. It is proposed that a voltage pulse may only propagate through a limited number of transistor stages and still be latched.

The proportion of all transients in combinational logic that were latched into registers was experimentally estimated to be between $0.7 \cdot 10^{-3}$ *and* $2 \cdot 10^{-3}$ *for a custom designed CMOS circuit. Very few multiple bit flips were observed during the experiments which indicates that the single bit flip model used in many high-level simulations is reasonable accurate.*

1 Introduction

Single Event Upsets (SEUs) caused by heavy-ion or α-particle radiation are an important class of transient fault effects in digital circuits. SEUs are bit errors in stored information which are caused by single ionizing particles. If such a particle pass through a depletion region in an integrated circuit it generates a voltage pulse, see [1] and [2], that may alter the information stored in one or several latches.

SEUs pose a major problem in space applications because on-board electronics are subjected to cosmic heavy-ion radiation. SEUs can also be caused by α-particles emitted from small amounts of radioactive elements in the silicon or the packaging material of an integrated circuit.

There are at least two ways in which particle induced voltage pulses may cause bit flips in latches: (i) the particle may hit a sensitive volume directly in a latch which immediately causes the latch to flip, or (ii) the particle may hit a sensitive volume in combinational logic generating a voltage pulse which propagates through sensitized paths in the combinational logic and eventually causes an erroneous bit value to be loaded into one or several latches. The first type of SEUs are dominating, even in circuits having most of their sensitive volumes in combinational logic, as direct hits in latches have a much higher probability of causing bit flips. Hits in the combinational logic, on the other hand, only cause bit flips if the voltage pulse arrives to a latch during the *latching window* [3], i.e. the time during which the voltage pulse can alter the bit value loaded into the latch. The latching window constitutes only a small fraction of the total time, and consequently the probability is low that a voltage pulse originating from combinational logic actually becomes latched. Furthermore, there must also exist a sensitized path from the affected node to a latch, otherwise the voltage pulse is *logically masked.*

This paper presents an experimental method for investigating the impact of particle induced transients in combinational logic in CMOS circuits. The main goal is to provide a method for estimating the probability that such transients propagate into memory elements. This probability is estimated using a model of the bit flip intensity caused by transients in combinational logic. The parameters in this model are determined by: (i) physical fault injection experiments using heavy-ion radiation from Cf-252, (ii) switch-level and circuit-level simulations, and (iii) general knowledge about the circuit investigated.

In the physical fault injection experiments, a novel technique is used to determine the relative frequency of SEUs originating from combinational logic and direct hits in latches, respectively. This technique is based on using two irradiation experiments, one in which the entire chip is irradiated, and one in which only some combinational parts are irradiated by shielding the rest of the circuit from the irradiation.

In our analysis we also consider the possibility that a transient pulse may be attenuated as it propagates through a combinational network. This phenomenon, which is referred to as *electrical masking*, has not previously been taken into account in the context of latching of transients.

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When designing and validating systems that must tolerant SEUs, it is important to know the proportion of SEUs that originate from combinational logic. An important problem in this context is that transients in combinational logic may propagate to several latches due to fan out in the logic network and, hence, may cause multiple bit flips. A recent study using simulation-based fault injection to investigate the SEU vulnerability of the ISCAS-89 sequential benchmark circuits, showed that more than ten percent of the latched voltage pulses originating from combinational logic caused multiple bit errors [3]. The results presented in this paper show a much lower overall proportion of multiple bit errors. This type of knowledge is important for validating error models used in RTL or gate-level simulation-based fault injection experiments. In the past, such experiments have been based mostly on the single flipped bit error model, see for example [4] and [5]. To analyze the effects of particle induced charge deposition in large integrated circuits various mixed-mode simulation strategies have also been proposed, [6] and [7]. A methodology for fast transient fault simulation based on fault dictionaries is presented in [8].

The target circuit used in the experiments is described in Section 2. Section 3 presents the bit flip intensity model. The experimental set-up and the results of the physical fault injection experiments are described in Section 4 and 5, respectively. In Section 6, specific parameters of the model are derived from simulations and the circuit layout. The estimation of the probability that transients in the combinational logic propagates into memory elements is presented in Section 7. Finally conclusions are given in Section 8.

2 Circuit description

A circuit of low complexity has been used in the experiments. The circuit was designed as a full custom circuit (as a part of an undergraduate course in VLSI design) and was manufactured by Austria Mikro Systeme International in an 1 μm CMOS process. The reason for using the circuit in the experiments is that the design and the process parameters of the circuit are known in detail.

The circuit is a Berger code checked program counter consisting of 2,372 transistors. The main part of the circuit is combinational but it also contains 40 master-slave flip-flops. Figure 1 shows the block diagram of the circuit.

The information symbol part (IS) of the program counter is processed in the information processor and the corresponding operation is performed on the check symbol part (CS) by the Berger processor. The Berger checker monitors the program counter and signals an error when there is a mismatch between the information part and the check symbol part. A Berger check symbol generator implemented as a tree of full adders, [9], is included in the

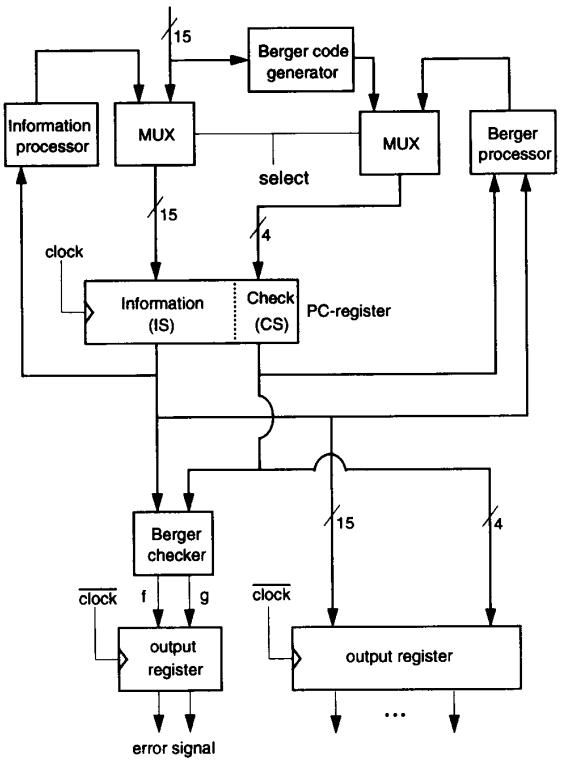

Figure 1 Block diagram of the test circuit.

Berger checker. The Berger processor includes combinational logic for counting the number of leading ones in the information symbol to predict the new check symbol value based on the previous check symbol. The two multiplexers shown in Figure 1 allow external initialization of the PC.

The Berger code checking scheme is capable of detecting any unidirectional multiple bit error in the PC-register. The network is aimed to be included as a subnetwork in a self-checking processor in which the checking circuitry not only checks a PC-register and an adder but also an entire register bank and data buses. The circuit has two large combinational blocks that are located separately which makes the circuit a suitable target for our physical fault injection experiments. The error detection capability of the circuit is not used for any specific purpose in the experiments. In fact, the Berger code checking circuitry is regarded as an ordinary functional block. In the physical fault injection experiments, however, all errors observed in the PC-register were detected by the checker which is to be expected as mostly single bit flips were obtained. The output registers are not necessary for the function of the circuit but are included to sample and buffer the results.

Figure 2 shows the floorplan. The complexity in terms of the number of transistors of the main building blocks is given within parentheses.

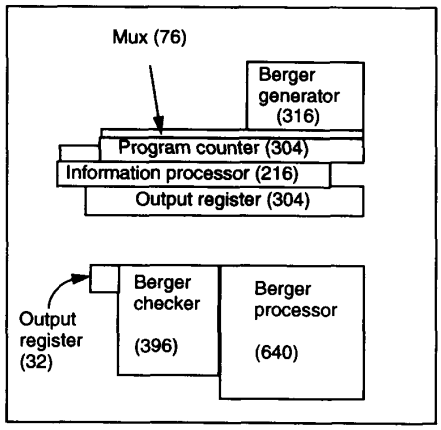

Figure 2 Floorplan and transistor count.

3 Modeling

There are many reasons why a voltage transient on a node in a combinational block may not propagate to the outputs of the block. In many situations there is no sensitized path from the affected node to the outputs. This is referred to as logical masking. Another reason for the pulse not to reach the outputs is that the duration or the magnitude of a pulse may decrease with the number of transistor stages it propagates through. When the duration (or magnitude) of the pulse is lower than a certain threshold value, the pulse can no longer propagate through a transistor and consequently it fades out. This phenomenon is referred to as electrical masking. One reason to introduce the hypothesis of electrical masking in this context is that circuit-level simulations have shown the possibility for a pulse only to pass a limited number of CMOS inverters in a chain.

The bit flip intensity of latched transients, λ_C, is modeled as a product of four parameters:

$$\lambda_C = \lambda \times N_{SC} \times P_{latch} \times P_{prop} \quad (1)$$

First, λ_C is direct proportional to the heavy ion intensity per pn-junction, λ. The second factor is the number of sensitive pn-junctions in the actual combinational network, N_{SC}. Third, we have the ratio between the width of the latching window and the register clock period, P_{latch}. The fourth factor is the probability that a voltage pulse propagates to a latch input, P_{prop}. In a previous gate-level investigation [3] this last factor considers the effect of logical masking, i.e. no sensitized path exists between the affected node and the latch. An additional modeling assumption in this paper is that we introduce the concept of electrical masking.

The bit flip intensity caused by direct hits in latches, λ_R, can be expressed as:

$$\lambda_R = \lambda \times N_{SR} \times P_{flip} \times P_{dc} \quad (2)$$

The heavy ion intensity, λ, is the same as in (1). N_{SR} denotes the number of sensitive pn-junctions in the latches. The third factor, P_{flip}, represents the proportion of sensitive pn-junctions in a latch that can lead to a bit flip. The last factor, P_{dc}, denotes the duty cycle of the latches, i.e. the proportion of time they hold a valid bit value. The parameters are summarized in Table 1.

As we have detailed knowledge of the experiment circuit, the parameters N_{SC}, N_{SR}, P_{flip} and P_{dc} can be determined without performing any physical experiments. This is done in Section 6. The intensities λ_C and λ_R can be estimated from two experiments. One in which direct heavy-ion hits in registers dominate (Experiment 1) and one in which latching of transients dominate (Experiment 2). Denoting the total experiment time T, and the number of observed bit flips N, these estimations can be expressed as:

$$\lambda_R^* = \frac{N_R}{T_R} \quad (3)$$

$$\lambda_C^* = \frac{N_C}{T_C} \quad (4)$$

It is reasonable to assume that over the chip area there is a uniformly distributed heavy ion intensity per pn-junction, λ. There are three main arguments for this assumption. First, all transistors are of the same size. Second, there is a uniformly distributed heavy-ion flux over the chip area. Third, the layout does not impose any systematic masking of the ions. This assumption makes it possible to relate the two experimental results to one another. This means that based on the experimental estimations of λ_C and λ_R and the assumptions about the values of N_{SC}, N_{SR}, P_{flip} and P_{dc}, it is possible to estimate the product $P_{latch} \times P_{prop}$, i.e. to what extent particle induced transients in combinational logic are latched into the registers:

$$P_{latch} \times P_{prop} = \frac{\lambda_C \times N_{SR} \times P_{flip} \times P_{dc}}{\lambda_R \times N_{SC}} \quad (5)$$

Section 7 includes estimations of the parameter P_{latch} and P_{prop}. Determining a value of P_{prop} gives us the possibility to quantify the effect of electrical masking, i.e. the possibility that a voltage pulse only can propagate through a limited number of transistor stages and still be latched.

Table 1 List of parameters.

λ	Heavy ion intensity per pn-junction.
λ_R	Bit flip intensity caused by direct hits in latches.
λ_C	Bit flip intensity of latched transients from combinational logic.
N_{SR}	Number of sensitive pn-junctions in the latches.
N_{SC}	Number of sensitive pn-junctions in the combinational logic.
N_R	Number of observed single bit flips during Experiment 1.
N_C	Number of observed single bit flips during Experiment 2.
T_R	Observation time of Experiment 1.
T_C	Observation time of Experiment 2.
P_{flip}	Proportion of sensitive pn-junctions in a register that can lead to a bit flip.
P_{dc}	Proportion of time (duty cycle) a latch contains valid data.
P_{latch}	Ratio between the width of the latching window and the register clock period.
P_{prop}	Probability that a voltage pulse propagates to a latch input.

4 Experimental setup

As the main goal is to investigate to what extent particle induced transients are latched into the registers, it must be experimentally possible to distinguish between errors caused by hits in the registers and errors caused by hits in the combinational parts. The approach chosen to reach this requirement is to use two different samples of the circuit, see Figure 3 and 4: one with the entire circuit area irradiated, Experiment 1, and one for which only two combinational blocks are exposed to heavy-ion radiation, Experiment 2. On the second sample all the chip area but two combinational blocks, the Berger processor and the Berger checker, is shielded with a 150 µm thick layer of shielding material. By adopting this strategy it is guaranteed that the observed bit flips in Experiment 2 are caused by latched transients.

For both experiments it is assumed that the heavy-ion intensity is uniformly distributed over the pn-junctions. The objectives of Experiment 1 are to estimate this intensity and to verify the assumption of uniformly distributed heavy-ion flux. In Experiment 2, the latching of transients originating from combinational logic is directly observable. Comparing the observed bit flip intensities in the two

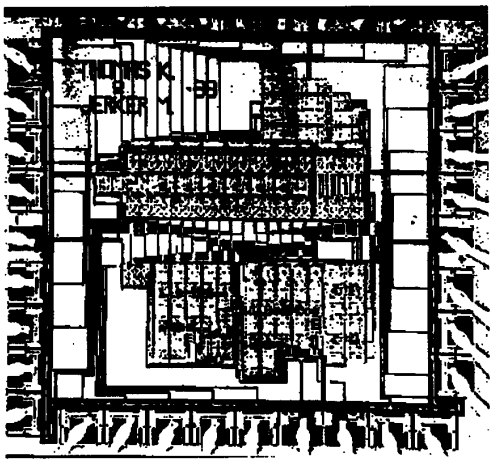

Figure 3 Unshielded chip sample.

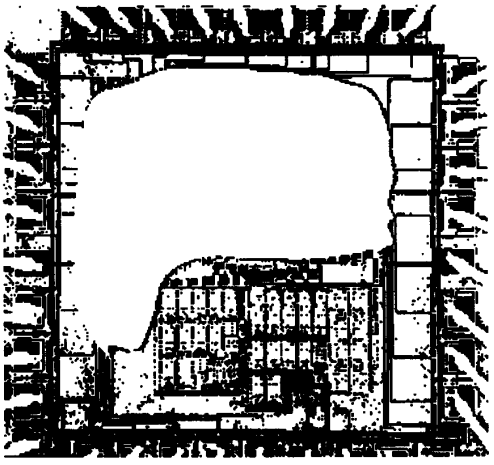

Figure 4 Shielded chip sample.

experiments in combination with some simulation results presented in Section 6, makes it possible to estimate the value of $P_{latch} \times P_{prop}$, i.e. to what extent particle induced transients in combinational logic are latched into the registers.

The spontaneous fissioning of Californium-252 is a practical source of highly energetic heavy particles. The use of Cf-252 as a fault injection method was described in [10] and is further reviewed in [11]. When a heavy ion penetrates the depletion layer of a reverse biased pn-junction, it deposits charge which induces a current pulse [1] locally at the pn-junction. This current pulse generates a voltage pulse [2] which may be manifested as an error in a register.

When an ion hits combinational logic the induced voltage pulse may propagate through the network to the inputs of a memory element. If the pulse arrives to the memory element at a time within the latching window interval of the cell, then the pulse will be latched into the register.

As heavy ions are attenuated by air molecules, the irradiation of the circuits must be performed in vacuum. In the experiments a miniature vacuum chamber [11] which can be handled freely without any special arrangements for radiation protection has been used. The time and location of fault injection cannot be controlled as the decay of the Cf-252 is a random process. By the use of the golden chip method (Figure 5), in which the circuit under test is synchronized and compared with an identical circuit not subjected to irradiation, the effects of the faults at the output pins can be observed.

The program counter in the circuit investigated is increased by one in an indefinite loop at a clock frequency of 5 MHz. A logic analyzer, which operates at the same speed, samples the output registers. From the observed errors it is possible to determine the type (flip-to-0 or flip-to-1) and the location of the internal bit errors caused by the heavy ions. The actual pn-junction of the heavy-ion impact can, however, not be determined.

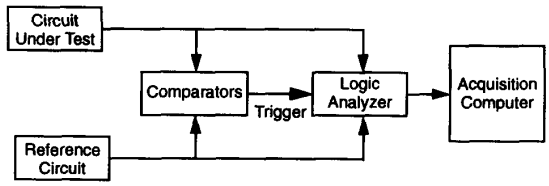

Figure 5 Block diagram of the experimental set-up.

Generally, for an unshielded circuit it is not possible to analyze whether the erroneous state emanates from a direct heavy-ion hit in a register or from a hit in the combinational part.

5 Experimental results

5.1 Unshielded chip (Experiment 1)

Table 2 shows the distribution of bit flips in the PC-register obtained in Experiment 1, i.e. with the entire circuit area exposed to heavy-ion radiation. As shown in Figure 1, the only registers in the target circuit are the PC-register and the output registers. Only bit flips in the PC-register are studied. A total of 613 bit flips were recorded. The total observation time was 112 hours. Consequently, the mean time between bit flips was about 11 minutes. A few multiple bit errors were observed in the experiment. However, these errors were originally caused by single bit flips which propagated through the adding circuitry of the information processor. This is further explained at the end of this section. Table 2 shows the distribution of the number of single bit flips obtained together with the estimation of the relative frequency of occurrence at a confidence level of 95%. As the PC-register contains 19 bits, the expected relative frequency of occurrence is $1/19 = 0.053$. This value is enclosed in almost all intervals. Thus, it is reasonable to assume that the probability of bit flips is approximately equal for all register bits.

Table 2 Distribution of bit flips in the PC-register.

	flip-to-0		flip-to-1	
Register	#	rel. freq. (95%)	#	rel. freq. (95%)
IS(14)	9	[0.010 , 0.046]	18	[0.034 , 0.089]
IS(13)	19	[0.033 , 0.085]	18	[0.034 , 0.089]
IS(12)	15	[0.024 , 0.070]	19	[0.037 , 0.093]
IS(11)	13	[0.019 , 0.062]	10	[0.013 , 0.055]
IS(10)	20	[0.036 , 0.089]	13	[0.021 , 0.068]
IS(9)	19	[0.033 , 0.085]	12	[0.018 , 0.064]
IS(8)	25	[0.049 , 0.108]	8	[0.009 , 0.046]
IS(7)	26	[0.051 , 0.111]	18	[0.034 , 0.089]
IS(6)	22	[0.041 , 0.096]	12	[0.018 , 0.064]
IS(5)	17	[0.028 , 0.078]	13	[0.021 , 0.068]
IS(4)	17	[0.028 , 0.078]	16	[0.029 , 0.081]
IS(3)	19	[0.033 , 0.085]	12	[0.018 , 0.064]
IS(2)	14	[0.021 , 0.066]	19	[0.037 , 0.093]
IS(1)	15	[0.024 , 0.070]	22	[0.045 , 0.105]
IS(0)	7	[0.006 , 0.038]	22	[0.045 , 0.105]
CS(3)	20	[0.036 , 0.089]	8	[0.009 , 0.046]
CS(2)	19	[0.033 , 0.085]	16	[0.029 , 0.081]
CS(1)	9	[0.010 , 0.046]	15	[0.026 , 0.076]
CS(0)	15	[0.024 , 0.070]	22	[0.045 , 0.105]
TOTAL	320		293	

To analyze the ratio of flip-to-0 and flip-to-1 bit errors the proportion of zeroes and ones in the register cells must be determined. The internal register cells of the circuit can be divided into 15 information bits and 4 Berger check bits. The program counter is increased by one in an indefinite loop. As the program counter runs through all combinations, it is obvious that the information bits have an equal proportion of zeroes and ones. The Berger check symbol is the bitwise complement of the binary representation of the number of ones in the information field (15 bits wide). As

there are equally many information words with k ones as there are information words containing 15-k ones, the Berger check bits have an equal proportion of ones and zeroes. The number of expected flip-to-0 and flip-to-1 bit errors are consequently equal.

In Table 3, the proportion of the total number of flip-to-0 and flip-to-1 errors have been estimated from the experimentally obtained relative frequencies of occurrence (Table 2). At a 95% level of confidence, it can be concluded that there is no major asymmetry in the proportion of the number of flip-to-1 and flip-to-0 errors.

Table 3 95% confidence intervals of the proportion of bit flips.

flip-to-0	flip-to-1
[0.482 , 0.562]	[0.438 , 0.518]

Although the first manifestation of an ion hit is a single bit error, multiple bit errors can be the first externally observable effect of the hit. The reason for this is the clocking strategy of the output register. The PC-register which consists of master-slave flip-flops, see Figure 8, has two phases of operation. During the first phase, when the clock input is high, the input value is written into the master latches. The contents of the master latches are then transferred to the slave latches during the second phase, i.e. when the clock is low. Consider the situation when a heavy ion causes a single bit to flip in the slave latch of the IS register during the first phase. The erroneous output of the IS register is increased by one and may therefore result in a multiple bit error being written into the master latches. In the second phase (clock is low) this multiple bit error is stored in the slave latches. The contents of the PC-register is sampled to the output register when the clock is low, and consequently this single bit flip manifests as a multiple bit error in the output register. In the experiments, 38 multiple bit errors of this type were observed. These faults were classified as single bit errors. The faulty bit was determined by subtracting one from the erroneous output.

5.2 Shielded chip (Experiment 2)

In Experiment 2, only the Berger processor and Berger checker are irradiated as shown in Figure 6. If these combinational blocks are further decomposed, the Berger processor has a 4-bit full adder as an output sub-block, and the Berger checker ends with a 4-bit two-rail checker. The registers are of standard CMOS master-slave type, see Figure 8. Table 4 shows the results of Experiment 2.

Table 4 Number of bit flips in the registers caused by latched transients from combinational logic.

check symbol (CS)		f and g output register	
# single bit	# mult. bit	# single bit	# mult. bit
16	2	5	0

Bit flips in the check symbol part of the PC-register are caused by the latching of transients originating from the Berger processor and bit flips in the f and g output registers are caused by transients in the Berger checker. The total observation time was 648 hours. The mean time between bit flips was about 28 hours.

In Experiment 1, the mean time between bit flips in the check symbol part (CS) was 54 minutes. The corresponding mean time in Experiment 2, when considering only transients originating from the Berger processor, was 2200 minutes. Therefore, it is reasonable to neglect the contribution of transients in combinational logic to the bit flip intensity in Experiment 1.

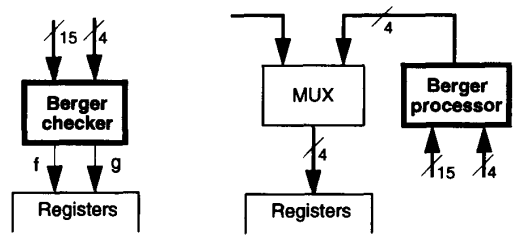

Figure 6 Irradiated combinational parts of the circuit (shaded).

6 Parameter estimations

In this section the propagation of voltage pulses in combinational networks is simulated. The proportion of voltage pulses that are likely to reach the outputs of the Berger processor and Berger checker is determined under various assumptions about the impact of electrical masking. From this, it is possible to estimate the probability, P_{prop}. Furthermore, the values of the parameters P_{flip}, P_{dc}, N_{SR}, N_{SC} are determined. The order of magnitude for P_{latch} is also determined.

To estimate the proportion of pulses that may propagate to the outputs of a combinational block, simulation-based fault injections were carried out. A modified version of the event-driven switch-level simulator described in [12] was used for transient fault injection. By injecting temporary state changes on nodes connected to a sensitive pn-junction, the simulator can trace the propagation paths of the injected state changes. Which of the drain/source regions

that are sensitive varies dynamically and is determined by the input vector and the previous state of the network. For a given input vector, all pn-junctions sensitive to charge deposition were subjected to fault injection. All logical masking effects are taken into account in these simulations. The simulator keeps track of the number of transistor stages a pulse must pass before it can reach a register input. A voltage pulse can pass through a transistor in two ways. First, a voltage pulse at the transistor gate terminal may cause the drain/source terminals of the transistor to transiently change its state. Second, a pulse at the drain/source terminal of a conducting transistor may propagate to the source/drain terminal. It is assumed that the attenuation of the pulse is equal for both types of signal propagation. Thus, both correspond to one transistor stage when determining the propagation length for a pulse. The effects on a pulse caused by the capacitive load of a node are not considered.

Table 5 shows the results of simulations when 800 randomly chosen input vectors were applied to the Berger processor and the Berger checker. The average number of the injected pulses that can propagate to the inputs of the latches are listed as a function of the assumed maximum number of transistor stages a pulse can pass. Logical masking is taken into account. For example, it can be seen that, in average, 50.7 faults propagate to the outputs of the Berger checker when only logical masking is considered (column "<∞"). With the assumption that a pulse originates at most 3 transistor stages away from a latch input (column "≤3") the corresponding number is 21.0, which is a significant decrease. Thus, the number of transients that may propagate to the outputs is strongly dependent upon the electrical masking effect. From Table 5 it is possible to estimate P_{prop} under various assumptions regarding electrical masking.

Table 5 Average number of the injected pulses that propagate to the inputs of a latch under different assumptions of the longest possible propagation path.

Block	Assumed distance in terms of number of transistor stages to a latch input that the pulse can pass and still be latched.									N *
	0	≤1	≤2	≤3	≤4	≤6	≤8	≤10	<∞	
Berger proc.	0	4.0	12.0	26.0	39.5	48.1	51.9	53.2	53.2	234
Berger checker	3.0	10.3	16.6	21.0	25.0	34.1	44.0	50.0	50.7	148

*N = Average no. of injected faults per vector.

The latching window of a register is the neighborhood of the clock edge for which a pulse of a given duration is latched [3]. In order to estimate the width of the latching window, circuit-level simulations of the register flip-flops were performed. The register flip-flops are of master-slave type and the master is transferred to the slave on the negative transition of the signal at the clock input. Figure 7 shows a timing diagram when a transient pulse is applied to the input of the register flip-flop. In the simulations the arrival time, t, of the pulse was varied to determine the width of the latching window.

It is assumed that the minimum rising and falling times of the clock pulse is 0.1 ns. The minimum voltage transient is assumed to have a duration of 0.5 ns and a rising and fall time of 0.1 ns. The simulations showed that the minimum latching window is about 0.5 ns.

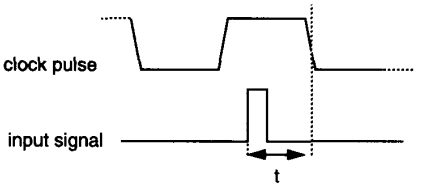

Figure 7 A pulse applied at the input of a register.

In a register cell, as seen in Figure 8, there is only some of the sensitive junctions that can actually flip the cell when hit by a particle. The number of sensitive pn-junctions connected to each node is given in the figure. Note that these numbers are constant, independent of the logic state of the cell. The total number of sensitive junctions in a master-slave cell is eleven. Circuit-level simulations of a current pulse applied to each of the nodes have been performed to model the effects of an ion hitting a sensitive region. The results showed that for a pulse of realistic width and magnitude (≤1 pC) a state change can occur only when node N_a and N_b are fault injected in the master and slave latches, respectively. Thus, there are only eight junctions in a cell that may cause a bit flip when hit by a particle. P_{flip} denotes the probability that a register cell changes its state (master or slave latch) given that a voltage transient has occurred. Thus, $P_{flip} = 8/11$ for these registers. Moreover, as each latch only holds its value during one of the two clock phases (it is transparent during the other) the probability, P_{dc}, that a state change is not overwritten during a clock cycle is 0.5.

N_{SR} is obtained by multiplying the number of register cells (19) with the number of sensitive pn-junctions in a register cell (11). N_{SC} is determined from the switch level simulations and is the average number of sensitive pn-junctions per input pattern. All estimated parameter values are given in Table 6.

Table 6 List of parameter values.

N_{SR}	Number of sensitive pn-junctions in the PC-register.	209
N_{SC}	Average number of sensitive pn-junctions in the Berger processor and the Berger checker.	382
N_R	Number of observed single bit flips during Experiment 1.	613
N_C	Number of observed single bit flips during Experiment 2.	23
T_R	Observation time of Experiment 1.	$4.0\ 10^5$ s
T_C	Observation time of Experiment 2.	2.310^6 s
P_{flip}	Proportion of sensitive pn-junctions in a register that can lead to a bit flip.	8/11
P_{dc}	Proportion of time a latch is not transparent.	0.5

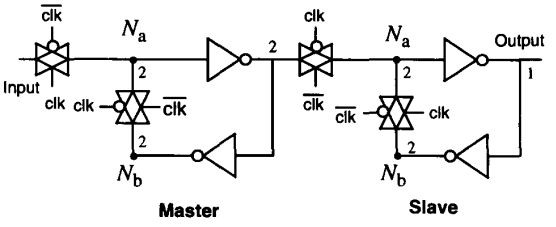

Figure 8 CMOS master-slave latch.

7 Analysis

7.1 Estimating the product $P_{latch} \times P_{prop}$

The product $P_{latch} \times P_{prop}$ is the proportion of all transients occurring in combinational logic that are latched into a register. This proportion can be calculated according to (5). The estimations of the bit flip intensities in (3) and (4), inserted into (5), result in:

$$(P_{latch} \times P_{prop})^* = \frac{N_C \times T_R \times N_{SR} \times P_{flip} \times P_{dc}}{N_R \times T_C \times N_{SC}} \quad (6)$$

A point estimation of (6) is obtained by inserting the values in Table 6:

$$(P_{latch} \times P_{prop})^* = \frac{23 \times 4.0 \cdot 10^5 \times 209 \times \frac{8}{11} \times 0.5}{613 \times 2.3 \cdot 10^6 \times 382} =$$

$$= 1.3 \cdot 10^{-3}$$

Next follows an analysis of the estimation accuracy.

In (5) the parameter values of N_{SR}, N_{SC} and P_{flip} are considered to be exact. The parameter P_{dc} is assumed to be very close to 0.5 as a consequence of the symmetric clock. Hence, the inaccuracy of the estimated product is dominated by the problem of estimating the intensities λ_C and λ_R, respectively.

A 96% confidence interval of the ratio between the two intensities can be guaranteed by first calculating 98% confidence intervals for λ_C and λ_R, respectively. Generally, the mean time to event, $1/\lambda$, can be estimated within an interval of a certain confidence. The 98% confidence intervals becomes:

$$I_{1/\lambda_c} = [6.5 \cdot 10^4, 1.7 \cdot 10^5] \quad \text{seconds}$$

and

$$I_{1/\lambda_R} = [6.0 \cdot 10^2, 7.2 \cdot 10^2] \quad \text{seconds}$$

This gives the 96% confidence interval of the ratio λ_C/λ_R:

$$I_{\lambda_C/\lambda_R} = [3.4 \cdot 10^{-3}, 1.1 \cdot 10^{-2}]$$

As all other parameters in (5) are considered being exact, a 96% confidence interval of the product $P_{latch} \times P_{prop}$ is given by:

$$I_{P_{latch} \times P_{prop}} = [6.8 \cdot 10^{-4}, 2.2 \cdot 10^{-3}]$$

Assuming no electrical masking, P_{prop} can be calculated from Table 5 as:

$$P_{prop} = \frac{53.2 + 50.7}{234 + 148} = 0.27$$

As the product $P_{latch} \times P_{prop}$ is known this corresponds to a latching window between 0.5 ns and 1.6 ns. The shorter a transient is assumed to be able to propagate through a combinational network, the wider the latching window has to be to correspond to the experimental results. Without determining the effects of electrical masking the experiments imply a latching window greater than 0.5 ns that is consistent with the simulation results in Section 6.

7.2 Experimental estimation of P_{prop}

In this section we estimate the effects of electrical masking, by interpretation of the second experiment only. The results in Section 6 show that the expected ratio between the number of latched transients from the two blocks varies with the assumptions concerning the electrical masking. If for example a transient pulse could not pass through any transistor stages, only transients occurring in the Berger

checker could be latched, see Table 5. In this case we would observe bit flips only in the f and g output registers. The reason for this is that the outputs of the Berger processor pass a shielded multiplexer before reaching the check symbol latches.

Let the number of observed bit flips in the check symbol part of the PC-register be denoted N_{CS}, and the bit flip intensity of latched transients in the check symbol register be denoted λ_{CS}. In Table 7, the expected proportion of bit flips in the check symbol part, λ_{CS}/λ_C, is listed as a function of the number of transistor stages a voltage pulse is assumed to be able to propagate and still be latched. It can be observed that as a consequence of the difference in structure between the two combinational blocks, this relation is not a monotonic function but rather have a maximum for about 4 transistor stages.

Table 7 The expected proportion of bit flips in the check symbol part, λ_{CS}/λ_C based on simulation.

	Assumed no. of transistor stages that the pulse can pass and still be latched.									
	≤0	≤1	≤2	≤3	≤4	≤5	≤6	≤8	≤10	<∞
λ_{CS}/λ_C	0	0.28	0.42	0.55	0.61	0.60	0.58	0.54	0.52	0.51

From the experiments we estimate the ratio of bit flips in the check symbol:

$$(\lambda_{CS}/\lambda_C)^* = N_{CS}/N_C = 18/23 = 0.78 \qquad (7)$$

This estimation is high in comparison with the expected proportion when a moderate degree of electrical masking (corresponding to the right most columns in Table 7) is assumed. This indicates that electrical masking may exist. Calculating the accuracy of this estimation we first observe that the number of observations is large enough to make the normal approximation.

A 99% one-sided confidence interval becomes:

$$\frac{\lambda_{CS}}{\lambda_C} > 0.56$$

So far it is likely to assume that a transient in average can pass somewhere between 4 and 7 transistor stages and still be latched. Hence, there is no reason from the experimental data to exclude the possibility that a pulse cannot pass a very large number of transistor stages.

8 Conclusions

This paper presented an experimental method for estimating the probability that particle induced transients in combinational networks propagate into memory elements. For the target circuit used in these experiments, this probability was estimated to be between $0.7 \cdot 10^{-3}$ and $2 \cdot 10^{-3}$. The method is based on two fault injection experiments, one in which the entire circuit is irradiated (Experiment 1), and one in which only some combinational parts are irradiated by shielding the rest of the circuit (Experiment 2).

In Experiment 2, two combinational blocks with different topologies and consequently different propagation properties were subjected to fault injection. By observing the proportion of bit flips in the output registers of each block, the number of transistor stages that the pulse can pass and still be latched can be determined. The width of the latching window can be determined by combining the results of the two experiments.

Experiment 1 showed that about 2% of the bit errors in the check bits of the PC-register were caused by latching of transients in combinational logic, i.e. 98% were caused by direct hits in these latches. The bit flips were approximately uniformly distributed over the register cells and there was no major difference in the number of flip-to-0 and flip-to-1 errors obtained.

Furthermore, in Experiment 1, no multiple bit error were observed and in Experiment 2, only two multiple bit errors occurred. This indicates that the single bit flip model used in many high-level simulations is reasonable accurate.

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