

A Study on the Utility of Using Expected Quality Level as a Design for Testability Metric

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Abstract

This paper develops a Physical Design for Test (PDFT) metric that is directly related to the expected quality level (QL) contribution of a cell to a circuit, and it details experimental results showing the usefulness of this metric in predicting the quality level contribution of a cell to circuits that have yet to be designed. The PDFT metric shows what QL increase can be expected for the circuit by changing the physical design of a component of the circuit.

1 Introduction

The purpose of physical design for test (PDFT) is to allow IC manufacturers to increase the quality of a shipped product; more formally, to increase the *quality level*, the fraction of shipped circuits that are fault-free. Traditional approaches to improving quality level have focused on ease-of-detection [4, 5, 11, 13], but the likelihood of occurrence of potential faults is also important: Physical design for test addresses both of these factors. PDFT entails modifying the physical layout of a circuit in order to shift the distribution of faults toward those having a greater chance of being detected. Since many design environments reuse logic units (those using standard cells or gate arrays, for example) and since faults internal to a cell can account for a significant percentage of circuit faults [6], PDFT of the logical units or cells is an efficient means for quality level enhancement.

Our PDFT methodology for logical units in a circuit requires information that can be obtained from the circuit topology, the physical design of the cell, and from the various components of the test environment [7]. This information can be used to develop a

measure of cell testability, which can in turn be used to judge the relative merits of different cell designs or, alternatively, to indicate which aspects of the physical design can be altered to improve testability. Because the improvement of quality level is the goal of any testing effort, quality level itself is the metric of choice for design, for testability. For cell PDFT, a good metric would be an estimation of the cell's contribution to the quality level of a circuit in which the cell will be used. The work of Jee and Ferguson [7] describes the PDFT methodology we are using, but we modify it by including the expected change in the quality level of circuits for which this PDFT method is used.

This paper presents a method for computing an estimation of the cell's contribution to quality level and uses this contribution as a metric for guiding the PDFT of the cell. Section 2 describes the terms that will be used throughout the paper, Section 3 introduces the PDFT metric, starting from the definition of quality level, and Section 4 describes the tools and methods we use for computing the metric. Section 5—the primary contribution in this paper—presents experiments detailing the ease of logic detection of various faults in cells embedded in the ISCAS circuits, and it discusses the implications on the feasibility of deriving the cell testability metric on one set of circuits and using that to predict the testability of other circuits using the cell. Finally, Section 6 presents the conclusions from our study.

2 Definitions

An important concept in the development of the PDFT metric is that of a *test environment*—not only the methods used for circuit testing, but any portion of the circuit specifically added to improve the detectability of faults. The testing method specifies how the circuit under test is stimulated and which parameters (logic levels, current, timing, etc.) are monitored to gauge the response to the stimuli. It is important to keep the test environment in mind when characterizing faults: when we state that a fault is de-

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tected or undetected in a circuit, the specification of a test set and detection criteria is implicitly assumed.

Defects are anomalies in the physical makeup of a circuit that may be due to many causes—among them are foreign particles, misaligned photolithographic masks, and scratches. A defect is *critical* when it produces a change in the electrical description of the circuit, such as the introduction of a resistor between two nodes that were intended to be isolated. This change is referred to as a *fault*. The changes in the electrical characteristics of the circuit that result from a fault constitute the fault’s *behavior*. For logic circuitry this may be a change in the truth table, in propagation delays across a logical unit, in the switching or quiescent current, or in any number of other circuit parameters. For a specific testing environment, however, only a few (often only one) of these types of behaviors are monitored.

The relationship between defects and faults is important for determining the probability that a fault will occur. Defects may occur in different layers of the physical circuit and may vary in size and shape. These defect properties determine which faults the defect may cause. For instance, a sufficiently large defect consisting of conducting material deposited in the metal layer may cause an electrical short between two otherwise isolated metal nodes. However, if the defect is smaller than the smallest distance between the nodes, the short will not be caused by this defect. A simple defect model capturing these qualities views the defect as either the presence of excess material or the absence of intended material in a given layer of a process. The defect’s shape can be modeled as a circle or square so that its size is characterized by a single length. With this view of a defect, we define the *critical area*, $C_{d,f}$, as the area of the circuit within which, if the center of a defect of type d falls, fault f results. For a uniform defect density, D_d , the expected number of defects of type d that would produce fault f is $C_{d,f}D_d$. Since many defect types may cause the same fault, the expected number of defects of *any* type that would produce fault f is given by the sum, $\sum_d C_{d,f}D_d$, where d ranges over all defect types (a type is specified by a combination of the properties constituting our defect model). This expected number is sometimes called the fault’s *weighted critical area* (WCA_f) [2], a convention we will also follow. The probability that a fault f with weighted critical area WCA_f occurs is $1 - e^{-WCA_f}$, when the defect densities are uniform¹. The gener-

¹Since, with a uniform defect distribution, the distribution of the number of defects from sample to sample is Poisson (the probability of having n defects = $\frac{\langle n \rangle^n e^{-\langle n \rangle}}{n!}$, with $\langle n \rangle$ the

alization to non-uniform defect distributions, which can account for defect clustering, is straightforward [8, 12], but the addition of a clustering parameter complicates the expressions, obscuring the concepts we wish to elucidate here; we therefore remain content with the assumption of uniformity.

3 Derivation of a PDFT metric

From a testability perspective, the redesign of a cell should be driven by the difficulty of detecting faults in the cell and by the probability that the faults occur. As previously mentioned, improved quality level is the goal of any organization that manufactures ICs, and so it is the goal of this work to incorporate the cell-redesign concerns into an appropriate testability measure. This section shows how a cell contributes to the quality level of a circuit in which it is embedded.

To reiterate, Quality Level (QL) is the fraction of shipped circuits that are fault-free. That QL is not 1 is a consequence of the incompleteness of the tests applied by the manufacturer; a circuit containing only faults that are not detected by the tests will be shipped. A good estimator for QL is the probability that a circuit that passes a set of tests is truly fault free. Our goal is to extract the contribution that a cell makes to a circuit’s quality level in terms of fault occurrence probabilities. The role that ease-of-detection plays in QL will fall out of the analysis. We begin by expressing the circuit’s QL in terms of these probabilities:

$$\begin{aligned} QL &= p(\text{fault-free} \mid \text{passes tests}) \\ &= \frac{p(\text{fault-free and passes tests})}{p(\text{passes tests})} \\ &= \frac{p(\text{fault-free})}{p(\text{passes tests})}. \end{aligned}$$

The last equality follows due to the assumption that any chip that is fault-free also passes the tests. For purposes of exposition, we represent the probability that no detected fault is present as $p(\text{NDFP})$ and the probability that no undetected fault is present as $p(\text{NUFP})$. Assuming independence of fault occurrences, and recognizing that the probability that a chip that passes the tests is equal to the probability that no detected fault is present, we may rewrite the

expected value of n), the probability of having no defects is $e^{-\langle n \rangle}$. The probability that f occurs is the probability of the occurrence of at least one defect that causes f , which is $1 - e^{-\langle n \rangle}$; or, substituting WCA_f for $\langle n \rangle$, it is $1 - e^{-WCA_f}$.

quality level as

$$\begin{aligned}
QL &= \frac{p(\text{no faults present})}{p(\text{passes tests})} \\
&= \frac{p(\text{(NDFP) and (NUFP)})}{p(\text{passes tests})} \\
&= \frac{p(\text{NDFP}) \cdot p(\text{NUFP})}{p(\text{passes tests})} \\
&= p(\text{NUFP}) \\
&= p\left(\bigwedge_{uf} \overline{O_f}\right) \\
&= \prod_{uf} p(\overline{O_f})
\end{aligned}$$

In the last line, O_f is the event that fault f occurs in the circuit, $\overline{O_f}$ is the event that it does not, and the conjunction and corresponding product are over undetected faults. This formulation of QL for non-equiprobable faults has been set forth previously by Corsi et al. [3]. In that paper the term *elementary yield* (Y_f) is applied to what we here represent by $p(\overline{O_f})$.

To show the cell dependence of QL , the above product will be broken into factors by cell type and fault type. Each fault in the circuit may be viewed as having a type, t , characterized by the type of cell containing the fault and the schematic change that the fault corresponds to within that cell type. With a uniform defect distribution, the probability that a given fault occurs depends only on the fault's type. That is, two faults in two separate instances of a cell type within a circuit will have the same probability ($p(O_t)$) to occur if they correspond to the same electrical fault in that cell type. This suggests a grouping of the factors in the expression for QL according to fault type; the undetected faults of type t contribute a factor $p(\overline{O_t})^{U_t}$ to the product, where U_t is the number of such faults. Grouping in this way, quality level may be written

$$QL = \prod_t p(\overline{O_t})^{U_t}.$$

The factors of this last expression may be further grouped according to the cell type that each fault type may be found in. For this it will be useful to name the set, $\mathcal{S}(C)$, of fault types that may occur in cell type C . Then

$$QL = \prod_C q_C,$$

with

$$q_C = \prod_{t \in \mathcal{S}(C)} p(\overline{O_t})^{U_t}.$$

The products may be taken over all cell and fault types, since U_t will be zero (and the contributing factor will be 1) for those factors that were not in the original expression.

The term q_C is the contribution from a cell type C to the QL of the circuit being studied. This factor has the same form as QL itself, though it should be interpreted slightly differently. The difference is that q_C has meaning only in the context of the circuit as a whole. It is essentially a quality level for cell type C , but the decision of whether a fault is detected is determined with respect to the entire circuit and the testing methods applied to it and not with respect to an isolated cell of type C . To characterize the contribution to QL from one instance of cell type C , it is appropriate to use the geometric mean of the contributions from all instances of that cell type. Letting I_C be the number of instances, the single instance quality level contribution from cell type C , $q_{C,1}$, is

$$q_{C,1} \equiv \sqrt[I_C]{q_C} = \prod_{t \in \mathcal{S}(C)} p(\overline{O_t})^{\frac{U_t}{I_C}}.$$

Using the expression relating WCA to fault occurrence probability, $q_{C,1}$ may be written

$$\begin{aligned}
q_{C,1} &= \prod_{t \in \mathcal{S}(C)} (e^{-\text{WCA}_t})^{\frac{U_t}{I_C}} \\
&= \prod_{t \in \mathcal{S}(C)} e^{-\text{WCA}_t \frac{U_t}{I_C}} \\
&= e^{-\sum_{t \in \mathcal{S}(C)} \text{WCA}_t \frac{U_t}{I_C}}
\end{aligned}$$

For small values of the exponent, this is the same as the metric developed in by Jee[6, 7].

4 Tools and method for PDFT

Previous work described a system for computing the metric described above for a given test environment [6]: This section provides a brief summary of the tools and methods necessary to present our new metric.

The original metric consists of a sum of products (in the exponent), the factors of which may be viewed as characterizing the circuit topology and fault types ($\frac{U_t}{I_C}$) and the cell's physical design (WCA_t). The method suggested by Jee and Ferguson [7] divides its work accordingly (Figure 1). Carafe [1] and CShort

[2] are used for cell characterization, while Nemesis [10] is used to characterize the circuit. Carafe uses the cell layout and a file containing defect distributions and produces a list of short circuit (or open) faults and their corresponding weighted critical areas. CShort invokes SPICE to simulate each fault, producing a modified truth table for each fault in the cell. Meanwhile, Nemesis performs fault simulation on the specified circuit for a set of faults that we call *single pattern faults* (SPFs). (These have been referred to as single input pattern pseudo faults[7].) The test vectors used by Nemesis constitute another portion of the testing environment. In our case, Nemesis was used in its single stuck-at ATPG mode to produce the test vectors. The information derived from these computations can be combined to produce the metric.

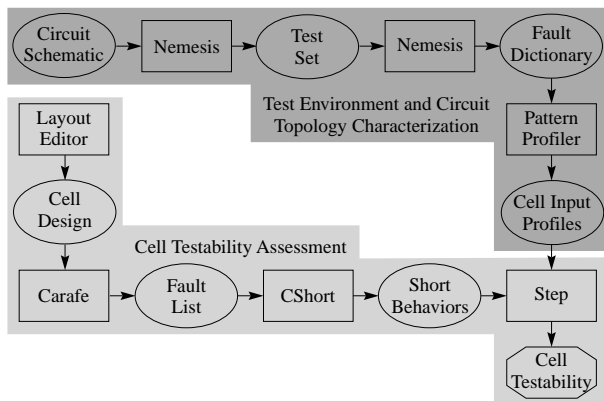


Figure 1: A data flow diagram of the implementation of the cell effective testability assessment procedure.

5 The utility of the metric

This paper focuses on the aspect of the metric derived from circuit topology. This is necessary to gain an understanding of the metric’s meaning in abstraction from the context of any particular circuit. The utility of the expression as written depends upon the generality of the factor $\frac{U_i}{I_C}$. For example, if this fraction is characteristic of the fault type only (for a fixed test environment), the quantity $q_{C,1}$ applies to a wide range of circuits and finds its maximum use as a metric. If, on the other hand, $\frac{U_i}{I_C}$ depends on some (topological) property of a circuit, $q_{C,1}$ only has meaning within a group of circuits sharing that property. If the property reflects a broad classification of functionality or some other easily determined similarity between circuits, the claim of cell-specificity of $q_{C,1}$

retains a high degree of validity, otherwise it does not. When $\frac{U_i}{I_C}$ depends significantly on the individual circuit for which it is computed, $q_{C,1}$ might as well be replaced by q_C , the full quality level contribution for that circuit. The generality of $\frac{U_i}{I_C}$ is really a question to be determined by experiment. In this section we attempt to gain insight into the matter by studying how $\frac{U_i}{I_C}$ varies within and between groups of circuits (in this case, the ISCAS85 and a combinationalized version of the ISCAS89 circuits) for a fixed testing method.

For this study, the schematics of the ISCAS89 circuits have been modified by changing the flip-flop outputs into circuit inputs and the flip-flop inputs into circuit outputs, and then removing wires that are inputs *and* outputs but do not affect the circuit in any other way. The ISCAS85 and ISCAS89 circuits are assumed to have differences in topological properties since the ISCAS89 circuits are modifications of sequential circuits that would presumably have significant differences in function from the ISCAS85 circuits. We also assume some common topological property exists within each circuit group. The tests applied are logic tests that have been generated by the Nemesis ATPG system to target single stuck-at faults.

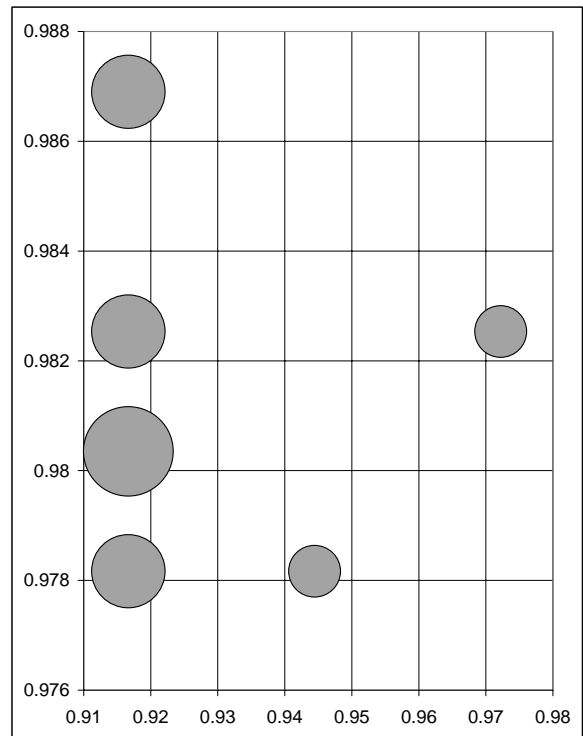


Figure 2: $1 - \frac{U_i}{I_C}$ for 1-SPF faults.

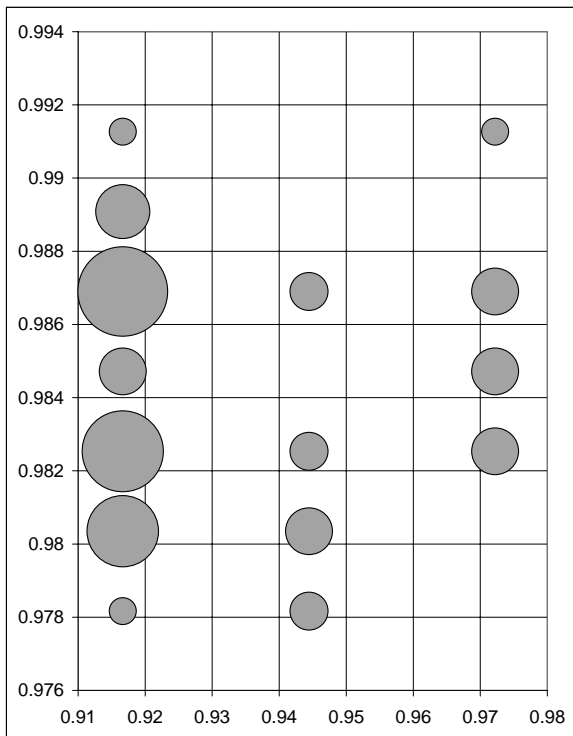


Figure 3: $1 - \frac{U_i}{I_C}$ for 2-SPF faults.

Since our goal is to determine how changes in the distribution of fault probabilities within a cell type changes the expected quality level of two sets of circuits, we will ignore how changes in the physical design of the circuit changes the distribution of faults within a cell and concentrate on how the potential faults in a cell affect that cell’s testability. More than one type of fault is possible in a cell, but we will assume that only a single fault can occur in a cell. In our experiment we will assume that two potential layouts exist for the cell and that the probability of a fault occurring in the two cells is equal (that is, they have the same WCA), but that the potential fault is different. The potential cell faults are defined by the single pattern faults (SPFs) they contain. We will also assume that the two faults for the two cells will contain the same number of SPFs.

For a single output cell, an SPF is equivalent to a discrepancy in a single row of the cell’s truth table; thus for an n -input gate there are $\binom{2^n}{k}$ faults with k SPFs. Although it is possible for defects that change the schematic of a cell to result in a 0 SPF fault, such faults will not be considered in this study.

5.1 Circuit groups correlations

In this section we explore the validity of applying the metric $q_{C,1}$ as computed using one set of circuits, to the cell C when used in a completely unrelated group of circuits. A strong correlation of $\frac{U_i}{I_C}$ between unlike groups of circuits would be evidence of maximum utility of $q_{C,1}$. To test for such a correlation, we investigated the value of $1 - \frac{U_i}{I_C}$ for the **nand4** gate in the ISCAS85 and ISCAS89 circuits². Remember that $\frac{U_i}{I_C}$ is the number of undetected faults of type t over the number of instances of the cell, and that since there is only one possible type of fault in this cell, this is the percentage of faulty cells that would have been detected by the test set produced by the ATPG program.

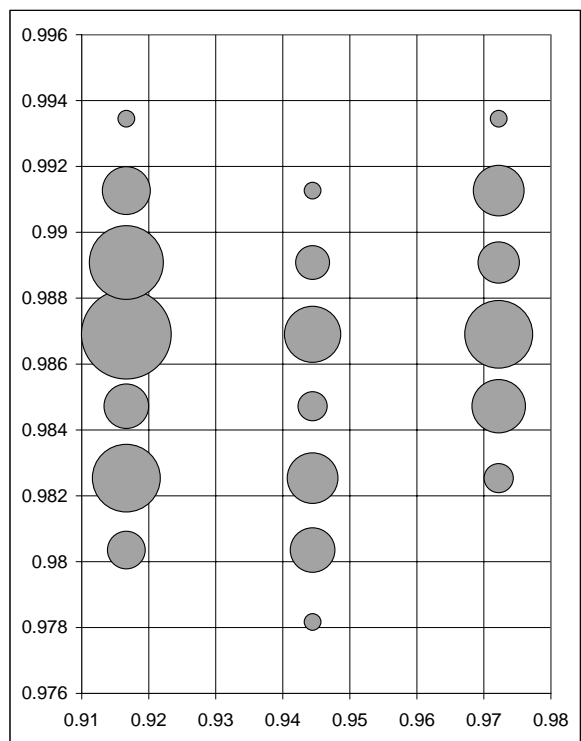


Figure 4: $1 - \frac{U_i}{I_C}$ for 3-SPF faults.

Figures 2 through 5 show $1 - \frac{U_i}{I_C}$ for for ISCAS85 and the ISCAS89 circuits: Each plot is a two dimensional histogram, with circle area proportional to the number of occurrences of the data point at the center of the circle, with the horizontal axis representing the ISCAS85 group values and the vertical axis representing the ISCAS89 group values. The largest circle,

²The **nand4** gate was chosen because first, there were a significant number of them in each of the two sets benchmarks and second, because the **nand4** has four inputs, there are 16 SPFs.

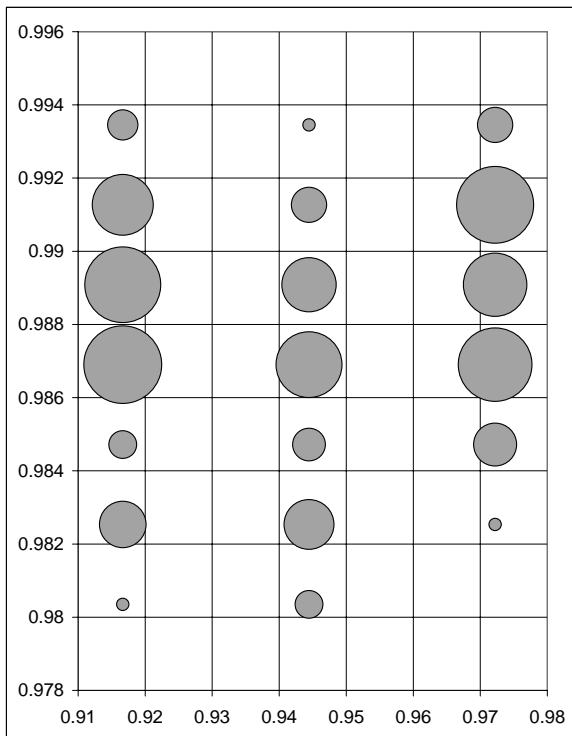


Figure 5: $1 - \frac{U_L}{I_C}$ for 4-SPF faults.

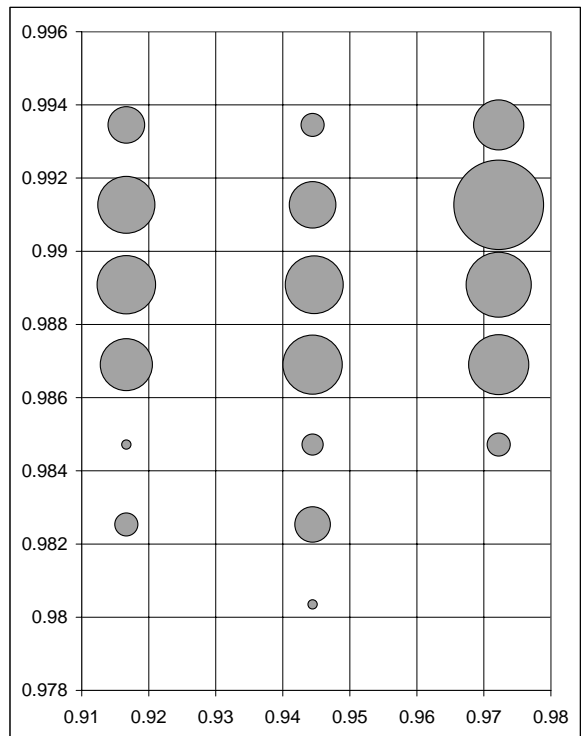


Figure 6: $1 - \frac{U_L}{I_C}$ for 5-SPF faults.

which corresponds to maximum detection in both circuit groups, has been removed because its dominant share of the area would have obscured the other data points. Note that for the ISCAS85 group there are only three values: the rightmost shows 35 of the 36 cell instances being detected, the middle shows 34 of 36 detected, and the leftmost shows 33 of 36 detected. Figure 2 displays the 16 faults consisting of one SPF, Figure 3 displays the 120 faults consisting of two SPFs, and Figures 4 through 6 similarly display three through five SPFs.

The statement we are trying to test is, “The detectability (D_{85}) of a given fault in the ISCAS85 group provides information about the same fault’s detectability (D_{89}) in the ISCAS89 group” or “ D_{85} is a good predictor of D_{89} and vice versa.” A perfect predictor would be a line “ $y = x$ ”. The qualitative evidence is that D_{85} is a poor predictor of D_{89} .

Because the a group of circuits within the ISCAS89 or within the ISCAS85 set are assumed to be more similar than a group of circuits with members from both the ISCAS89 and ISCAS85 groups, the results indicate that $q_{C,1}$ as a predictor of quality level is, at best, meaningful only within subgroups of circuits with some similar functional or topological properties. How such subgroups are defined is still an open

question, and clearly the metric would be of greater utility if an engineer does not have to go to too much trouble to define a group of similar circuits. Until significant correlation of detectability is demonstrated within a group of circuits, there is no justification for assigning an *average* value to the detectability of a group of circuits and using that value to predict an improvement in quality level for another group of circuits.

The next best hope would be that *changes* in detectability would be in the same direction (of the same sign) in both groups. If so, one could at least claim that improvement of a cell for a given circuit group is likely to either improve or not change the detectability of the cell in the other circuits with unrelated function (or topological properties). The plots in Figures 7 through 11 show the results of such a comparison. For each plot, the change in $1 - \frac{U_L}{I_C}$ from one fault to another with the same number of SPFs is plotted for both the benchmark groups. The largest data point, representing two faults with the same $1 - \frac{U_L}{I_C}$ and falling on (0, 0),³ is excluded to expose the more interesting cases. Points falling in the

³Such points correspond to no change in detectability for either group and are therefore neutral with regard to the question at hand.

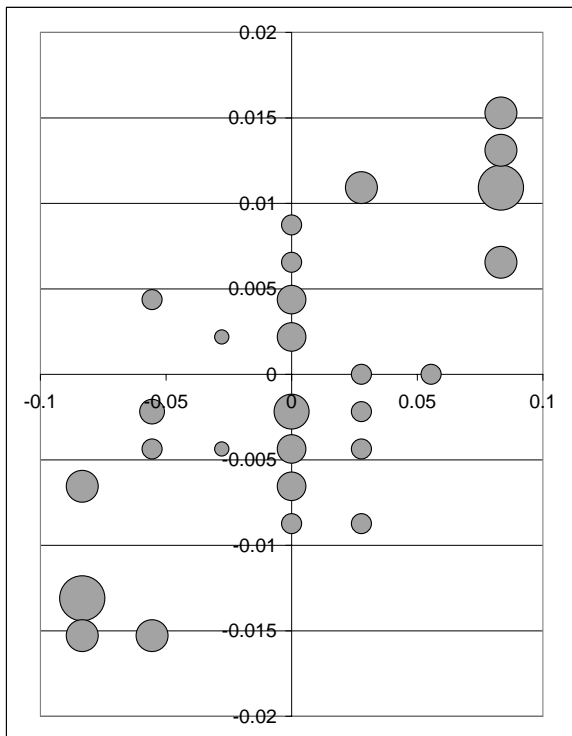


Figure 7: Change in $1 - \frac{U_L}{I_C}$ for 1-SPF faults.

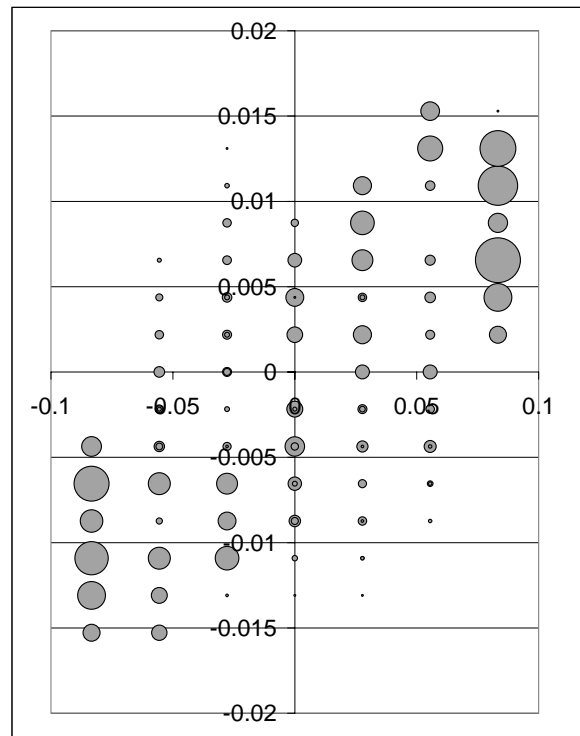


Figure 8: Change in $1 - \frac{U_L}{I_C}$ for 2-SPF faults.

upper-right or lower-left quadrants represent cases in which a change in faults improves or makes worse $1 - \frac{U_L}{I_C}$ in both groups, and points falling in the quadrants II and IV represent cases in which a change in faults improves $1 - \frac{U_L}{I_C}$ in one group and makes it worse in the other group. The strong clustering of points around the slope-1 line clearly indicates that improvements in the testability of a group of circuits, caused by changing the physical design of the cell to change the distribution of faults in that cell, will likely result in an improvement in the testability of another group of circuits using that cell.

The approach to PDFT that we have been following is useful for predicting changes in quality level if we accept the more restricted role for the metric. We arrived at the quantity $q_{C,1}$ with the expectation of a somewhat universal value of $\frac{U_L}{I_C}$. If we revert instead to the quantity, q_C , we have an estimation of the cell's contribution to quality level for a specific circuit. This can be used for building testability into an evolving design: different component cell designs can be compared on the basis of their likely quality level contribution to the circuit; no claim is made on the degree of improvement of a cell except in relation to the circuit considered.

In addition, as suggested previously by Jee, faults

that are undetectable with the current test environment may still lead to problems in some untested behavior, such as signal propagation or quiescent current, so they cannot necessarily be ignored. If we shift their critical area to faults that can be detected, any circuit using the revised cell will see an improvement in testability (if a tradeoff must be made, the question of which undetectable fault to address can be decided based on weighted critical area). There is, admittedly, a dilemma here since we are suggesting trading a fault with potential consequences or subtle faulty behavior with another that has certain, and easy to detect, consequences; this strategy errs on the side of reliability and quality level of the tested product⁴.

6 Conclusions

A primary goal of the present work has been to gain a perspective on the goals of improving cell testability, primarily through PDFT. With the recognition that the motivation for such improvements is always to increase quality level, our approach was to develop a method for estimating the effect of the cell design

⁴A similar debate rages concerning I_{DDQ} testing.

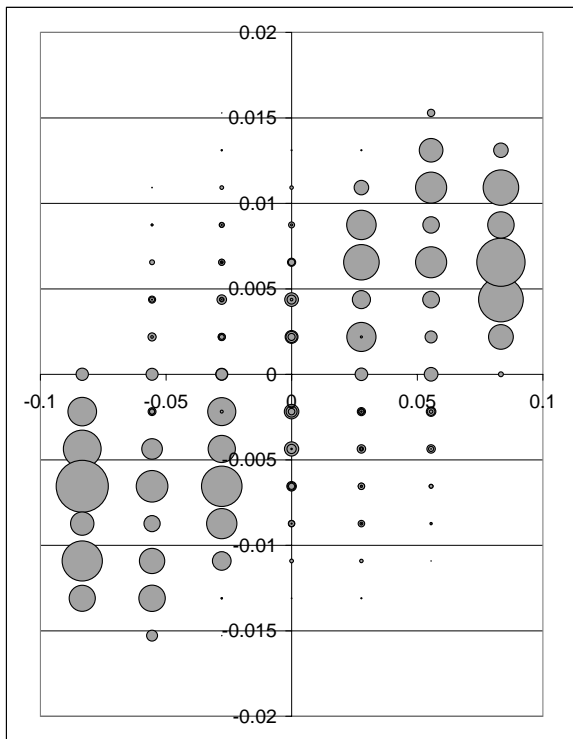


Figure 9: Change in $1 - \frac{U_c}{I_c}$ for 3-SPF faults.

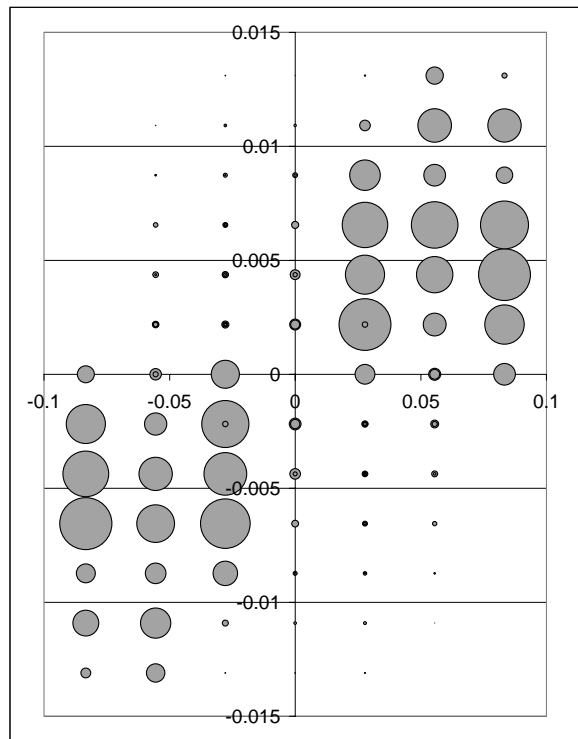


Figure 10: Change in $1 - \frac{U_c}{I_c}$ for 4-SPF faults.

on the chip’s quality level at the cell library design stage. This paper presented a quality metric for use during the physical design of a family of circuits that is based on a number of assumptions (the equation for $q_{C,1}$). To explore the utility of this metric, we chose two very different groups of circuits, a set of combinational benchmark circuits and a set of sequential benchmark circuits, and compared the average testability of the four input `nand` gate with different fault distributions for both circuits.

Our experiments showed that these testability values had far too little correlation to use this equation to predict the improvement in Quality Level, but that an improvement in the testability of the cell in one group of circuits will almost always lead to either an improvement in the testability in a very different group of circuits or no change in testability. So even though one cannot predict the quality level improvement due to a change in the physical design of the cell, one can determine with high confidence it will improve the quality level.

Finally, the authors wish to point out that the four input `nand4` gate was chosen for this experiment because a large number of logic faults can be simulated for it. Notably, simple gates, such as `nands` and `nors`, will not have as many reasonable changes

(that will significantly alter the distribution of faults) to the physical design as more complex gates will: More complex cells are necessary for the application of PDFT to be meaningful. Flip-flops, latches, and memory cells have a rich enough physical design space that changes in their physical design will result in many different faults in the different designs—especially true when one includes timing faults that are more subtle and sophisticated in these circuits—and these cells will provide a rich source for PDFT analysis and application.

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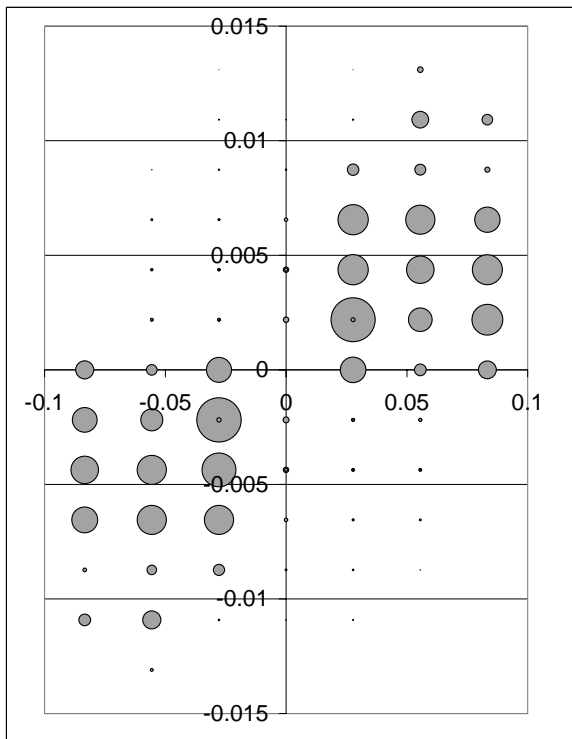


Figure 11: Change in $1 - \frac{U}{I_C}$ for 5-SPF faults.

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