

Guest Editors' Introduction:

Practical Asynchronous Design

IT GIVES US GREAT PLEASURE to present this special issue on asynchronous circuits and systems. The recent surge of interest in asynchronous circuits came about after an increase in VLSI communication applications and the current push toward achieving higher performance at lower power and design cost. Most of the recent literature on this topic, however, comes from academia and tends to be quite theoretical for practicing engineers. We wanted to concentrate on the practical aspect of various asynchronous circuits and systems.

Most industries dealing with circuits are designing asynchronous circuits, but such design is almost an art, with a significant portion of the knowledge gathered through learning on the job. We deliberately searched for articles from practicing designers and engineers to get the real picture of the state of the art in asynchronous circuit design and test. We wanted to achieve the following through the publication of this special issue:

- bring to the attention of the design community the advantages and disadvantages and the obvious and subtle differences between asynchronous and synchronous design techniques

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- bring to the attention of the research community the obstacles in taking asynchronous design to widespread acceptance, as well as a set of representative systems to enhance the system perspectives for research in asynchronous areas

We received 23 very high-quality submissions for this special issue, and we selected five for this issue. Six others will appear in following issues.

This issue features three articles from industry and two from academia. The latter two are practice-oriented, discussing actual chips designed and implemented to verify several theoretical issues and establish the design methodology of asynchronous circuits on a firmer footing.

From industry, we have authors Alan Marshall, Bill Coates, and Polly Siegel of Hewlett-Packard Laboratories, whose research indicates that asynchronous design has the potential to realize low-power implementations for some ap-

plications. Asynchronous design lets us 1) build circuits that can be electrically static while being ready for immediate operation, and 2) easily operate different parts of a system at different speeds to match local processing requirements.

Kees van Berkel, Ronan Burgess, Joep Kessels, Marly Roncken, Frits Schali, and Ad Peeters of Philips Research Laboratories and the Eindhoven University of Technology describe a complete DCC error corrector that consumes only 10 milliwatts. The unusually low power consumption results from a fully asynchronous implementation in which the energy waste of clock distribution, transients, and overhead of centralized control could be eliminated. The authors automatically compiled the chip, consisting of 155,000 transistors, from high-level descriptions.

Researchers from Philips Research Laboratories, Wolfgang Budde, Hans-Georg Keller, Hans-Jürgen Reumerman, and Paul van de Wiel, describe a practical implementation of building blocks of an ATM (asynchronous transfer mode) switch. They used the Mentor GDT design environment to achieve a top-down approach to design from a multilevel behavioral description. They produced the chip in a 1.0-micron

CMOS process and tested it to be fully functional up to a frequency of 100 MHz. This design is not purely asynchronous, but it gives a good picture of synchronous and asynchronous circuits being designed together.

Takashi Nanya, Yoichiro Ueno, Hiroto Kagotani, Masashi Kuwako, and Akihiro Takamura of the Tokyo Institute of Technology give details of the design and implementation of a general-purpose asynchronous microprocessor. They established a library of building blocks for design automation of asynchronous VLSI systems.

José A. Tierno, Alain J. Martin, Drazen Borkovic, and Tak Kwan Lee from the California Institute of Technology discuss circuit techniques for constructing delay-insensitive building blocks for asynchronous RISC microprocessors. One of the microprocessors reportedly runs at over 100 MIPS with a power consumption of 2 watts.

Among the six articles scheduled to appear in future issues is an invited article by Robert F. Sproull, Ivan E. Sutherland, and Charles E. Molnar, "Counterflow Pipeline Processor Architecture." These authors propose a radically new microarchitecture for RISC processors in which instructions and results flow in opposite directions in a self-timed pipeline.

Scott Hauck, Steven Burns, Gaetano Borriello, and Carl Ebeling of the University of Washington have enhanced field programmable gate arrays, the new implementation medium for digital circuits, to implement asynchronous circuits. Their article describes Montage, the first FPGA to explicitly support asynchronous circuit implementation, and its mapping software.


Trevor Lee, Mark Greenstreet, and Carl-Johan Seger in "Automatic Verification of Asynchronous Circuits" discuss using ordered binary decision diagrams for rigorous verification of asynchronous circuits. In one of their examples, their method found an error

that went unnoticed during more than 50 hours of CPU time simulation.

Victor Varshavsky, Vyacheslav Marakhovskiy, and Vadim Smolensky describe a procedure for designing a self-timed nonautonomous device by a finite automaton model. Two example cases considered by the authors produced good circuit solutions.

A.V. Yakovlev, A.M. Koelmans, and L. Lavagno present a formal design methodology, amenable to automation, for realization of interface logic. By dividing the design methodology into two stages—abstract synthesis and logic synthesis—they employ hierarchical decomposition of the initial implementation until its size can be handled by available logic synthesis tools.

Ganesh Gopalakrishnan proposes a new architectural idea that micropipelines can be realized in spatial dimensions. The author designed several example circuits using one- and two-dimensional micropipeline structures, and both ordinary C and LOCK elements.

THE ARTICLES SELECTED for this important topic are really at the cutting edge of practice in asynchronous design. You should get a good feeling for the way various institutions and laboratories are designing asynchronous circuits today and the emerging trends in the field. 

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