

Design of On-Line Testing for SoC with IEEE P1500 Compliant Cores using Reconfigurable Hardware and Scan Shift

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Abstract

In this paper, a new design for online testing of System on a Chip (SoC) is presented. The proposed method is based on usage of the available IEEE P1500 architecture and a small embedded FPGA core. Our method has a little additional routing overhead of the SoC, which will keep its performance much higher than conventional approaches. The design of this method is easy and it does not make a burden on the system designer. The error latency has an order of only few minutes in worst case scenario. We present the hardware implementation of this method and evaluate its performances.

1. Introduction

The usage of SoC is one of main issues that today researchers in Safety Critical Systems Design(SCSD) are investigating [1][3]. The system should be designed to capture error within relatively short time and eventually overcome it. Recently, some researchers investigated the usage of one unique embedded field programmable gate array to emulate all these cores, which they named heterogeneous redundancy [2]. When a fault occurs, it will be easily detected by comparing the results of the real core and an emulated core by analyzing the output responses. This method has the advantage of a SoC design for online testing and fault tolerance. It has an additional advantage of using only one output pin to flag a faulty chip. However, this method needs additional serious routing overhead which cause the degradation of the performance. Additionally, the design of this architecture make a burden on the system designer.

In this paper, our main target is to achieve the online fault detection of IEEE P1500 standard compliant core-based SoC with the least impact on the normal usage of the chip in terms of speed and design which is the problem of

the previous method [2].

One very attractive point of our testing approach is sharing IEEE P1500 architecture with online testing to minimize the designing cost of online testing architecture and the performance degradation caused by additional hardware and routing for the implementation.

2. Proposed Method

The basic idea in this paper consists of using IEEE P1500 architecture of each core for online testing of the SoC. In this method, we assume that the FPGA core can completely emulate all core function at the speed of the FPGA clock. The FPGA core is assumed faulty free. An illustration example is shown in Fig.1. This example contains three cores out of FPGA core. These cores have IEEE P1500 architecture. Therefore, each I/Os of each core is equipped with wrapper boundary cell. WSI/WSO (Wrapper Serial Input/Wrapper Serial Output) of all cores except WSI of core 1 and WSO of core 3 are connected to WSO/WSI of its adjacent cores. WSO of core 3 is connected to FPGA core. WRCK (Wrapper Clock) of all cores within the system are connected to FPGA clock. When we consider the testing of core 1 within the normal SoC operation, the test flow is as follows. Step 1, the FPGA core is configured to emulate the function of core 1. Step 2, the inputs/outputs data of core 1 are captured to the wrapper boundary registers. Step 3, the WSI and WSO of core 2 and core 3 are connected through WBR (Wrapper Bypass Register). Step 4, the data of core 1 are shifted into the FPGA core. The input data is sent to the input of the emulated core, and the output data is sent to the XOR tree input. The output of emulated core and the shifted output data of the real core are compared by the XOR tree. If a fault occurs, it will be easily detected by the outputs of XOR. Other cores are tested same as core 1. As shown in Fig.1, the FPGA core is configured to implement the serial to parallel circuit, one of the func-

tions of the core under test and XORing tree. Only one I/O pin will be necessary for FAIL/PASS signal, which would be activated if fault occurs. The fault is assumed here to be stuck at.

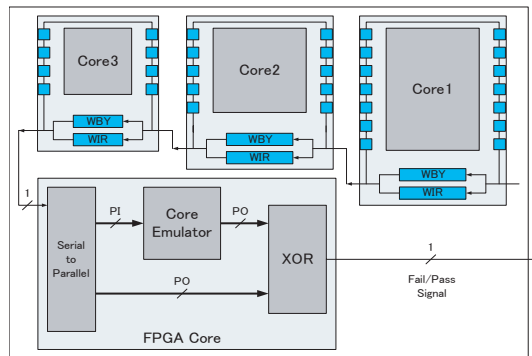


Figure 1. Basic structure of the proposed method.

3. Evaluation

The evaluation of this method will be performed in terms of the error latency metrics and routing overhead metrics.

3.1. Error Latency

One of the most important factors in SCSD is to design the system which is able to capture an error within relatively short time and eventually cover it when it occurs. Therefore, the error latency, which is defined as the mean time between the fault occurrence and its initial activation as an error, is very important metrics in SCSD.

Table 1. Minimum error latency.

	f_{conf} (MHz)			
	6	64	128	400
L (s)	87.6	80.6	79.7	78.8

Table 1 shows the value of this minimum error latency L of each configuration clock f_{conf} . From this results, failure is detected only within a few minutes. In this evaluation, we assume that our SoC cores are circuits from s38417, s35932, s15850, s9234, s5378, c7552, c6288 and c5315, which are relatively larger ISCAS benchmark circuits additionally to a single FPGA core.

3.2. Routing Overhead

Table 2 shows the routing overhead (RO) following the SoC size. The 1st column N is the number of the system

cores which construct the SoC, the 2nd column is the routing overhead of the conventional method[2], the 3rd is that of the proposed method and the 4th column represents the ratio of the routing overhead between the method [2] and the proposed method. From this table, we deduce that the routing overhead of our method is only 0.37 of the conventional one. We conclude that our method is better than the conventional method with respect to routing overhead.

Table 2. $N - RO$ specification

N	RO		
	[2]	Proposed	Proposed/[2]
8	2433	9	0.003699137
9	2689	10	0.003718855
10	2945	11	0.003735144
11	3201	12	0.003748828
12	3457	13	0.003760486
13	3713	14	0.003770536
14	3969	15	0.003779289
15	4225	16	0.003786982
16	4481	17	0.003793796

4. Conclusions

In this paper, we proposed a new online fault detection method using embedded FPGA core and IEEE P1500 architecture with the least impact on the normal usage of the chip in terms of speed and design, which makes the proposed method overcome the routing overhead which is the drawback of the previous method and reduce its hardware overhead compared to previous works. Additionally, the proposed online testing has valid error latency, which has an order of minutes in the worst case scenario.

References

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