

# **AN EFFICIENT SUCCESSIVE ELIMINATION ALGORITHM FOR BLOCK-MATCHING MOTION ESTIMATION**

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## **ABSTRACT**

Low power VLSI video compression processors are in high demand for the emerging wireless video applications [1]. Video compression processors include VLSI implementation of a motion estimation algorithm. Many motion estimation algorithms are found in the literature. Some of them are fast but can not guarantee an optimal solution; they can be stuck in a local optima. Such algorithms are fast, consumes less power when implemented in VLS, but they can result in high levels of distortion that cannot be accepted in many applications [1], [2], and [3]. On the other hand full search block matching algorithm (FSBM) is computationally intensive and a VLSI implementation of such algorithm has high power consumption [1], [4]. This paper presents an exhaustive search algorithm for block matching motion estimation. The proposed algorithm reduces the computational load with successive elimination of non-candidate blocks in the search window. Our proposed algorithm assigns each pixel to a category depending on its value. The number of categories is predetermined. The algorithm consists of number of stages, the first of which has the fewer categories, eliminating those search points that are the farthest from the match. The last stage is the FSBM but with fewer search points. This computational reduction leads to low-power VLSI implementation of the algorithm. Also, it leads to faster efficient motion estimation procedure. The correctness of this algorithm and its complexity are proved.

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